Datashee

APM32F003x4/x6

32-bit MCU based on Arm® Cortex®-M0+

Version: V1.1

1. Product characteristics

Systems Architecture

- 32-bit Arm® Cortex®-M0++core
- The maximum working frequency is 48MHz
- AHB bus, APB bus

Power, clock and reset

- Power supply voltage is 2.0~5.5V
- Clock: built-in factory calibrated 48MHz high-speed clock, built-in factory calibrated 128KHz low-speed clock, and external 1MHz-24MHz crystal oscillator
- Reset: power-on reset and power-down reset

Memories

- Up to 32Kbytes Flash
- Up to 4Kbytes SRAM

Low power consumption mode

- Support three low power consumption modes: wait, active-halt and halt

I/O

- Up to 16 I/O, all of which can be mapped to external interrupt controllers

Timer and PWM

- Two 16-bit advanced timers with 4-channel capture comparison function, PWM complementary output and dead time control
- 1 16-bit general timer, which supports PWM mode and 3-channel capture comparison function
- 1 8-bit basic timer
- Two watchdog timers
- 1 system tick timer
- 1 automatic wake-up timer

ADC

- 1 12bit resolution, 8 external channels, supporting differential input

communication interface

- 3 USART
- 1 I2C
- 1 SPI

1 BUZZER

Serial wire debugging SWD interface

Chip package

- TSSOP20/QFN20/SOP20

96-bit UID

Application field

- Smart home
- Medical equipment
- Motor driver
- Industrial sensor
- Auto parts

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2. Brief introduction

The APM32F003x4/x6 series chips are 32-bit microcontrollers based on Arm®Cortex®-M0+core, with the highest working frequency of 48MHz.

AHB high performance bus and APB advanced peripheral bus are embedded in the product. AHB high-performance bus can be combined with high-speed memory to realize fast data processing and storage; APB advanced peripheral bus can expand rich peripherals and enhanced I/O, and ensure the rapidity of connection and flexibility of control.

The product is embedded with 32 KB Flash and 4 KB SRAM, and has a 16-bit general timer, two 16-bit advanced control timers, an 8-bit basic timer, two watchdog timers, a system tick timer and an automatic wake-up timer. Product communication interfaces include: 1 I2C interface, 1 SPI interface and 3 USART interfaces. In addition, it also includes an ADC interface and a BUZZER interface. See APM32F003x4/x6 product function and peripheral configuration table for peripheral resources corresponding to specific models.

The working voltage of the product is 2.0~5.5V, and it has three different packages of TSSOP20/QFN20/SOP20. the peripherals and I/O configurations of different packages are different.

For information about the Arm®Cortex®-M0+core, please refer to the Arm®Cortex®-M0+technical reference manual, which can be downloaded from ARM’s website.

3. Function description

See the following table for specific APM32F003x4/x6 product functions and peripheral configuration.

Table 1 The APM32F003x4/x6 product functions and peripheral configuration

Products		APM32F003x4/x6					
		F4P6	**F6P6**	**F4U6**	**F6U6**	**F4M6**	**F6M6**
Encapsulation		TSSOP20	TSSOP20	QFN20	QFN20	SOP20	SOP20
Flash(Kbytes)		16	32	16	32	16	32
SRAM(Kbytes)		2	4	2	4	2	4
Timer	Advanced（16bit）	2					
	General (16bit)	1					
	Basic (8bit)	1					
	SysTick (24bit)	1					
	WUPT	1					
	WDT	2					
Communication Interface	USART	3					
	I2C	1					
	SPI	1					
12bit ADC	unit	1					
	channels	8					
GPIOs		16					
BUZZER		1					
Core		Arm®Cortex®-M0+					
Frequency		48MHz					
Service voltage		2.0~5.5V					

3.1. Core

The Arm®Cortex®-M0++core is built into the product, and the working frequency is 24MHz, which is compatible with mainstream ARM tools and software.

The system block diagram of APM32F003x4/x6 series chips is shown in Figure 3.

3.2. Memory

See the following table for details of memory:

Table 2 Memory description

Memory	Max bytes	Function
Built-in Flash	32Kbytes	Used to store programs and data.
Built-in SRAM	4Kbytes	It can be accessed in bytes, half words (16 bits) or full words (32 bits).

3.3. Power management

3.3.1. Power supply scheme

Table 3 Power supply scheme

Name	Abbreviation of name	Voltage range
Main power supply	V_{DD}/V_{SS}	2.0~5.5V
Analog partial power supply	V_{DDA}/V_{SSA}	2.4~5.5v

The V_{DD}/V_{SS} pin can supply power to the internal main voltage regulator (MVR) and the internal low power voltage regulator (LPVR), and the outputs of these two regulators together provide 1.5V power supply (V_{15}) to the core, Flash and SRAM.

3.3.2. Power supply monitor

Two circuits of power-on reset (POR) and power-down reset (PDR), are integrated inside the product. The two circuits are always in working state, ensuring the normal operation of the system when the power supply exceeds 2V.

When the power supply voltage is monitored to be lower than the specified threshold value $V_{POR/PDR}$, the system keeps the reset state without an external reset circuit.

See 8. Electrical Characteristics for details of $V_{POR/PDR}$.

3.3.3. Low power consumption mode

The product supports three low power consumption modes: Wait mode, Halt mode and Active Halt mode, which can be switched between these modes by setting, as shown in the following table:

Table 4 Low power consumption mode

Mode type	description
The Wait mode	– In the wait mode, the contents of all registers and RAM remain unchanged, and the previously defined clock (master clock state register CLK_CMSR) configuration also remains unchanged. – When an internal or external interrupt request is generated, the CPU wakes up from the wait mode and resumes working.
Halt mode	– In halt mode, the contents of all registers and RAM remain unchanged, and the configuration of clock (master clock status register CLK_CMSR) remains unchanged by default. – In this mode, in order to save power consumption, the main voltage regulator is turned off, and only the low voltage regulator (and power-down reset) is in working state. – HIRC starts up faster than HXT (see electrical characteristic parameters in data manual). Therefore, in order to reduce the wake-up time of MCU, it is recommended to select HIRC as the clock source of f_{MASTER} before entering pause mode.
Active halt mode (Active halt) mode	– Active halt mode is similar to halt mode, but it does not require external interrupt wake-up. It uses WUPT to generate an internal wake-up event after a certain delay, and the delayed time can be programmed by the user. – In default status, the main voltage regulator is active and can

Mode type	description
	wake up quickly from active halt mode, but its current consumption cannot be ignored. – In active halt mode, fast wake-up can reduce the response time of CPU and make the switching time between MCU running state and low power consumption mode shortest.

3.4. Clock

The four clock sources HXT, HXT user-ext, HIRC and LIRC can be the master clock, as shown in the following table:

Table 5 It can be used as the clock source of the master clock

Clock source	**description**
HXT	1-24MHz high speed external crystal oscillator
HXT user-ext	Maximum 24MHz high-speed external clock signal
HIRC	48MHz high speed internal RC oscillator
LIRC	128KHz low speed internal RC oscillator

Each clock source can be turned on or off independently to optimize power consumption. In order to make the system start quickly, the clock controller automatically uses HIRC's divide by 8 (HIRC/8) as the master clock after reset. The reason is that the stabilization time of HIRC is short, and the HIRC/8 can ensure the safe start of the system under poor V_{DD} conditions. Once other clock sources are stable, the user program can switch the master clock to another clock source.

3.5. Interrupt controller

3.5.1. Nested Vector Interrupt Controller (NVIC)

The APM32F003x4/x6 series chips are embedded with a nested vector interrupt controller, which can handle up to 23 masked interrupt channels (excluding Cortex®-M0+interrupt lines) and 4 priorities.

Nested Vector Interrupt Controller (NVIC) has tightly coupled NVIC interface, which can directly transmit interrupt vector entry address to kernel, and can

achieve low-latency interrupt response processing. In addition, it can give priority to high-priority interrupts, automatically save processor state, and automatically recover when interrupts return, without extra instruction overhead.

The module provides flexible interrupt management with minimal interrupt delay.

3.5.2. External interrupt controller (EINT)

The external interrupt controller includes four edge detectors for generating interrupt requests. Each interrupt line can be independently configured with trigger events and can be individually shielded. All I/O pins have external interrupt capability, and each port has an independent interrupt vector.

3.6. Timer

The product includes two advanced control timers (TMR1 and TMR1A), one general timer (TMR2), one basic timer (TMR4), two watchdog timers, one system tick timer and one automatic wake-up timer.

3.6.1. Advanced control timer (TMR1 and TMR1A)

Advanced timer functions are shown in the following table:

Table 6 Advanced control timer

Timer type	**Advanced control timer**	
Timer	TMR1	TMR1A
Counting resolution	16 bits	16 bits
Counter type	Up, down, up/down	Up, down, up/down
Prescaler coefficient	Any integer between 1 and 65536	Any integer between 1 and 65536
Capture/ Comparison Channels	4	4
Complementary output	Yes	Yes

Timer type	**Advanced control timer**
Function description	– Control the synchronous mode of timer with external signal – When the braking signal appears, the timer can be forced to output to a specific state – Two complementary outputs and software controllable dead time channels – Encoder mode – Interrupt source: 4 input capture/output comparison, 1 overflow/update and 1 brake signal interrupt This is a high-end timer, which is suitable for various control applications. Its complementary output, dead-time control and center-aligned PWM functions make its application fields extend to motor control, lighting and half-bridge driving modes.

3.6.2. General timer (TMR2)

General timer functions are shown in the following table:

Table 7 General timer

Timer type	**General timer**
Timer	TMR2
Counting resolution	16 bits
Counter type	Up
Prescaler coefficient	Exponential power of 2 between 1 and 32768
Capture/ Comparison Channels	3
Complementary output	-
Function description	Use external signal to control timer and synchronization circuit interconnected by timer Interrupt generation event: - Update: the counter overflows upwards, and the counter initializes (via software) - Input capture - Output comparison

3.6.3. Basic timer (TMR4)

The basic timer functions are as follows:

Table 8 Basic timer

Timer type	Basic timer
Timer	TMR4
Counting resolution	8 bits
Counter type	Up
Prescaler coefficient	Exponential power of any 2 from 1 to 128
Capture/ Comparison Channels	0
Complementary output	-
Function description	– Used to connect with external signals or cascade timers. – Interrupt generation. [When the counter is updated (the counter overflows) and when the trigger signal is input]

3.6.4. Watchdog (WDT)

Two watchdogs (independent watchdog and window watchdog) are embedded in the product, which can be used to detect and solve faults caused by software errors, thus improving the system security. The following table shows the comparative data of two watchdogs.

Table 9 Watchdog (WDT)

Name	Counter Resolver	Counter type	Prescaler coefficient	Function description
Independent watchdog	8 bits	down	Between 4 and 256 Any exponential	– It is driven by an internal independent 128kHz LIRC

Name	Counter Resolver	Counter type	Prescaler coefficient	Function description
(IWDT)			power of 2	RC oscillator as a clock source, so it still works as usual even if the master clock fails. – The whole system can be reset in case of problems. – You can provide timeout management for applications. – It can be configured as a software or hardware startup watchdog.
Window watchdog (WWDT)	7 bits	down	-	– Used to detect software faults, when it happens is generated by external interference or unexpected logic conditions, which causes the application to abandon its normal sequence. – Driven by the master clock, it has early interrupt warning function. – It can be configured as a software or hardware startup watchdog.

3.6.5. System tick timer (SysTick)

System tick timer is a standard 24-bit down counter with automatic reloading function. When the counter is 0, it can generate a masked system interrupt and

can program the clock source (HCLK or HCLK/8).

3.6.6. Automatic wake-up timer (WUPT)

WUPT can provide an internal wake-up time reference when MCU enters low power Active Halt mode. The clock of the time reference is provided by the internal low-speed RC oscillator clock (LIRC) or the pre-divided HXT crystal oscillator clock.

3.7. communication interface

3.7.1. 12C bus

Embedded with an I2C interface, it is led out through data pin (SDA) and clock pin (SCL), and can turn on or interrupt disable. It can work in multi-master mode or slave mode, supports 7-bit and 10-bit addressing, and allows connection to standard (up to 100kHz) or fast (up to 400kHz) I2C bus. I2C can receive and send data, convert serial data into parallel data when receiving, and convert parallel data into serial data when sending.

I2C bus functions are as follows:

Table 10 I2C bus function

Name	description
I2C main function	Generate start and end clocks
I2C slave function	Programmable I2C address detection Stop bit detection
Other functions of I2C	General generation and detection of 7-bit /10-bit addressing Support different communication rates: – Standard speed (up to 100KHz) – The fastest speed (up to 400KHz)

3.7.2. Universal asynchronous transceiver (USART)

Embedded with three USART communication interfaces, USART interface can support 1Mbit/s communication rate, and it has SPI emulation, high-precision baud rate generator, smart card emulation, IrDA SIR codec, LIN main mode and single-line half-duplex mode.

Table 11 Communication mode of universal asynchronous transceiver

Communication mode	**description**
Asynchronous communication (USART mode)	Full duplex NRZ standard format communication (mark/space)
	Programmable transmission and reception baud rate is up to 1Mbit/s, which can follow any standard baud rate at input frequency
	Independent enable bits for sending and receiving
	There are two wake-up modes: address bit (MSB) and idle line (interrupt)
	Transmission error detection and interrupt generation
	Parity control
Synchronous communication	Full duplex synchronous transmission
	SPI main operation
	8-bit data communication
	Maximum speed: 1mbit/s at 16MHz (fcpu/16)
LIN main mode	Transmit: generate a 13-bit synchronous interrupt frame
	Receive: detect an 11-bit interrupt frame

3.7.3. Serial peripheral interface (SPI)

Embedded with an SPI interface, it allows the chip to communicate with external devices in half/full duplex serial mode. It can be configured as master mode or slave mode, with 8 bits per frame. Full-duplex and half-duplex communication rates can support 8 mbit/s. SPI interface has wake-up function.

Table 12 Characteristics of serial peripheral interface

Characteristics	**description**
Maximum speed	Master/slave 8Mbit/s($f_{MASTER/2}$)
Full duplex synchronous transmission	Synchronous transmission is transmitted on two data lines with or without bidirectional transmission
Master-slave operation with two choices	Hardware or software
CRC calculation	-

Tx and Rx buffers	1 byte
Slave/master select input pin	-

3.8. Analog/digital converter (ADC)

ADC is a 12-bit successive comparison analog-to-digital converter, which can provide 8 multifunctional external input channels and 1 internal channel. channels AIN0~AIN7 come from IO channel, while channel AIN8 comes from on-chip VREF_BUFFER (a relatively stable standard voltage of 1.5V). ADC supports differential input mode in addition to single-ended mode, but channel AIN8 only supports single-ended input mode.

The analog watchdog function allows one channel, multiple channels or all selected channels to be monitored very accurately. When the monitored signal exceeds the preset threshold, an interrupt will be generated.

Events generated by the advanced control timer (TMR1) can cascade trigger ADC respectively, and applications can synchronize AD conversion with clock.

Table 13 ADC product features

Product features	**description**
Input voltage value	0 to V_{DDA}
Conversion mode	Single, continuous and buffered continuous conversion mode
Buffer	Size (10x12 bits)
Conversion channel	9, which can be converted once or continuously
Differential input	Four pairs
Analog watchdog	Programmable upper and lower limits of analog watchdog
Analog watchdog interrupt	Convenient handling of analog watchdog events
External trigger input	It can be triggered by a rising edge event on the ADC_ETR pin
Triggered from TMR1 TRGO	Yes
End of conversion interrupt	Settable

3.9. General purpose input/output port (GPIO)

16 GPIO pins are embedded, which can switch between input (pull-up, floating), output (push-pull, open drain) or multiplexing functions. Most GPIO pins are shared with multiplexed peripherals. In addition, some pins have redefined functions, such as analog input, external interrupt, and input/output of chip peripherals, but only one function can be mapped to a pin at the same time. The remapping of multiplexing functions can be realized by controlling option bytes. Please refer to the description of option bytes in the data manual.

3.10. BUZZER (Buzzer)

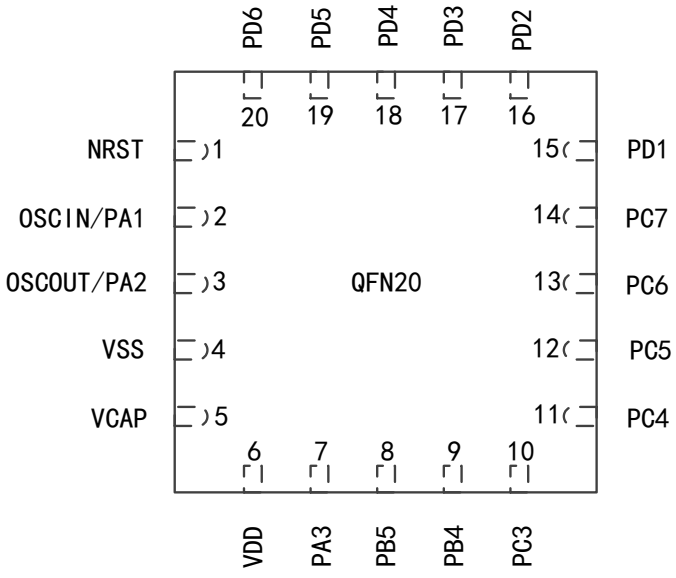
Embedded with a buzzer, when the LS clock works at 128kHz, it can generate a buzzer signal with frequency of 1kHz, 2kHz or 4kHz.

4. Pin characteristics

4.1. Pin definition

4.1.1. APM32F003x4/x6 series QFN20

Figure 1 Pin configuration diagram of QFN20



4.1.2. TSSOP20 and SOP20 of APM32F003x4/x6 series

Figure 2 Pin configuration diagram of TSSOP20 and SOP20

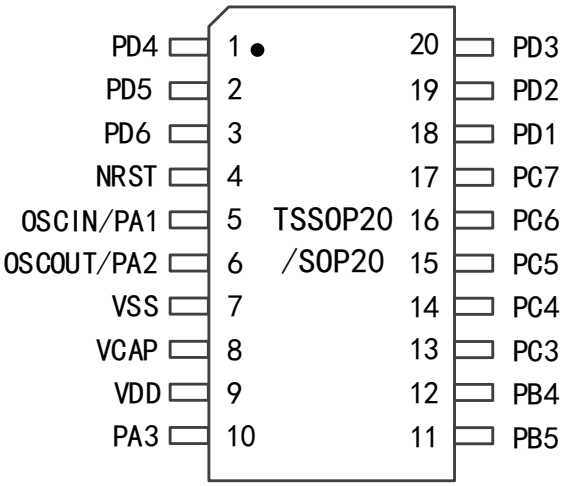

PD4 1
PD5 2
PD6 3
NRST 4
OSCIN/PA1 5
OSCOUT/PA2 6
VSS 7
VCAP 8
VDD 9
PA3 10
20 PD3
19 PD2
18 PD1
17 PC7
16 PC6
15 PC5
14 PC4
13 PC3
12 PB4
11 PB5
TSSOP20
/SOP20

Table 14 Pin definition of APM32F003x4/x6(20PIN)

Pin number			Pin name	Type (1)	Input			Output				Function after reset	Redefining functions
TSSOP20	SOP20	UFQFPN20			floating	wpu	Ext.interrupt	High sink	Speed	OD	PP		
1	1	18	PD4 BUZZER TMR2_CH1 USART1_CK TMR1A_CH2	I/O	X	X	X	HS	O3	X	X	PD4	-
2	2	19	PD5 AIN5 USART1_TX TMR1A_CH3 VAIN2 [TMR1A_CH1N]	I/O	X	X	X	HS	O3	X	X	PD5	TMR1A_CH1N [AFR5]
3	3	20	PD6 AIN6 USART1_RX TMR1A_CH4 VAIP2 [TMR1A_CH2N]	I/O	X	X	X	HS	O3	X	X	PD6	TMR1A_CH2N [AFR5]
4	4	1	NRST	I/O	-	X	-	-	-	-	-	Reset	-
5	5	2	PA1 OSCIN(2)	I/O	X	X	X	-	O1	X	X	PA1	-
6	6	3	PA2 OSCOUT	I/O	X	X	X	-	O1	X	X	PA2	-
7	7	4	V_{SS}	S	-	-	-	-	-	-	-	-	-
8	8	5	V_{CAP}	S	-	-	-	-	-	-	-	1.5V regulat/capacitor	-

Pin number			Pin name	Type (1)	Input			Output				Function after reset	Redefining functions
TSSOP20	SOP20	UFQFPN20			floating	wpu	Ext.interrupt	High sink	Speed	OD	PP		
9	9	6	V_{DD}	S	-	-	-	-	-	-	-	-	-
10	10	7	PA3 TMR2_CH3 TMR1_ETR USART3_CK [SPI_NSS]	I/O	X	X	X	HS	O3	X	X	PA3	SPI_NSS [AFR1]
11	11	8	PB5 I2C_SDA USART3_RX [TMR1_BKIN]	I/O	X	-	X		O1	T	-	PB5	TMR1_BKIN [AFR4]
12	12	9	PB4 I2C_SCL USART3_TX [ADC_ETR]	I/O	X	-	X		O1	T	-	PB4	ADC_ETR [AFR4]
13	13	10	PC3 TMR1_CH3 AIN7 VAIN3 [TLI] [TMR1_CH1N]	I/O	X	X	X	HS	O3	X	X	PC3	TLI [AFR3] TMR1_CH1N [AFR7]
14	14	11	PC4 TMR1_CH4 CLK_CCO AIN2 VAIP1 [TMR2_CH2N]	I/O	X	X	X	HS	O3	X	X	PC4	TMR2_CH2N [AFR7]
15	15	12	PC5 SPI_SCK AIN0 VAIP0 [TMR2_CH1]	I/O	X	X	X	HS	O3	X	X	PC5	[TMR2_CH1] [AFR0]
16	16	13	PC6 SPI_MOSI AIN1 VAIN0 [TMR1_CH1]	I/O	X	X	X	HS	O3	X	X	PC6	TMR1_CH1 [AFR0]

Pin number			Pin name	Type (1)	Input			Output				Function after reset	Redefining functions
TSSOP20	SOP20	UFQFPN20			floating	wpu	Ext.interrupt	High sink	Speed	OD	PP		
17	17	14	PC7 SPI_MISO [TMR1_CH2]	I/O	X	X	X	HS	O3	X	X	PC7	TMR1_CH2 [AFR0]
18	18	15	PD1 SWD USART2_CK TMR1A_CH1	I/O	X	X	X	HS	O4	X	X	PD1	-
19	19	16	PD2 AIN3 SWCLK USART2_RX TMR1A_BKIN VAIN1 [TMR2_CH3]	I/O	X	X	X	HS	O3	X	X	PD2	TMR2_CH3 [AFR1]
20	20	17	PD3 AIN4 TMR2_CH2 ADC_ETR USART2_TX TMR1A_ETR VAIP3	I/O	X	X	X	HS	O3	X	X	PD3	-

Note:

(1) I= input, O= output, S= power supply

(2) X: initial state after reset

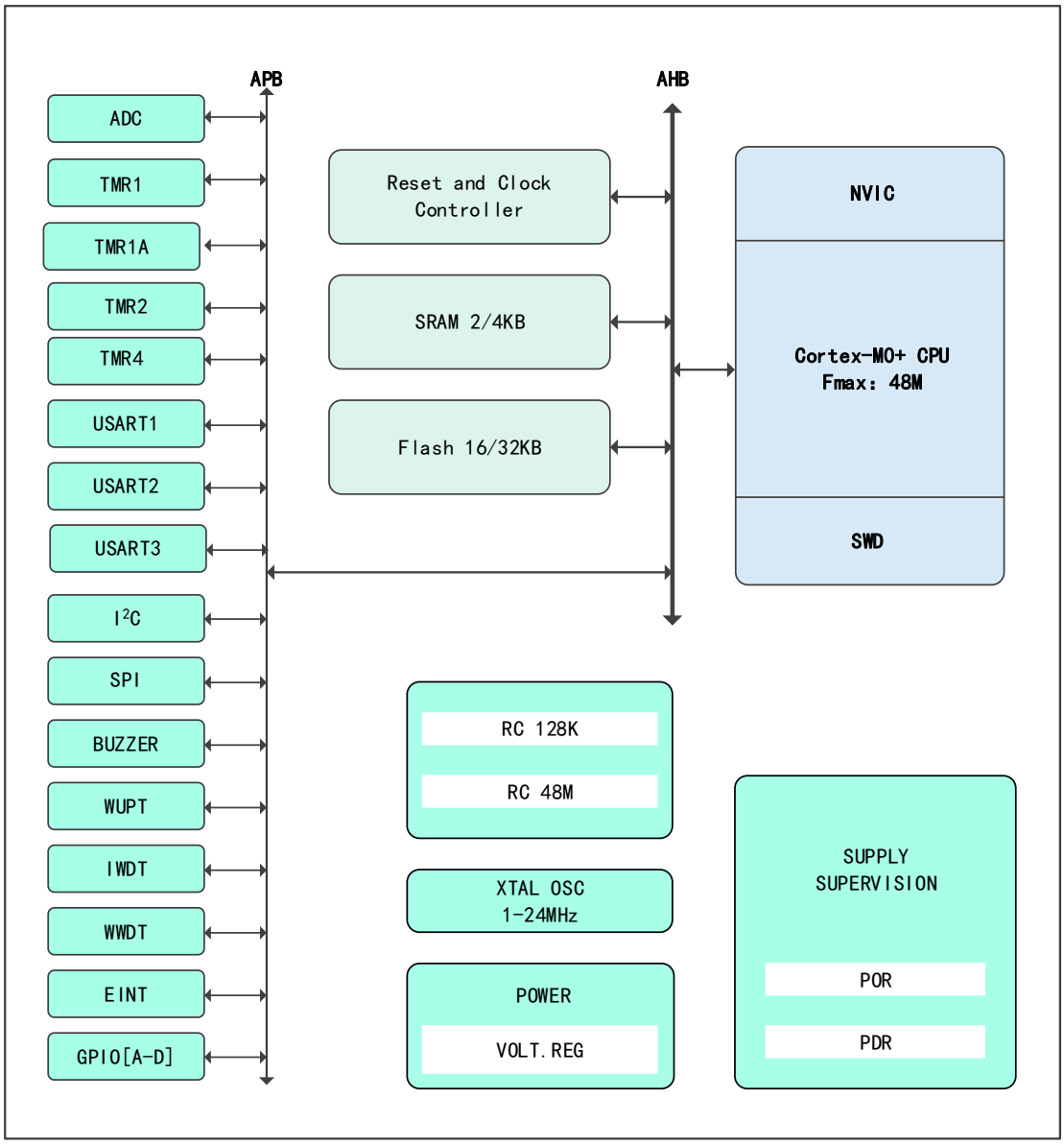
(3) T: true open drain I/O

(4) Floating= high resistance, HS= maximum sink current, OD= open drain, PP= push pull, wpu= weak pull up

(5) Speed: O1 = low speed, maximum 2m; O2= high speed, up to 10M；; O3= compatible with high and low speed, low speed at startup; O4= Compatible with high and low speed, high speed at startup

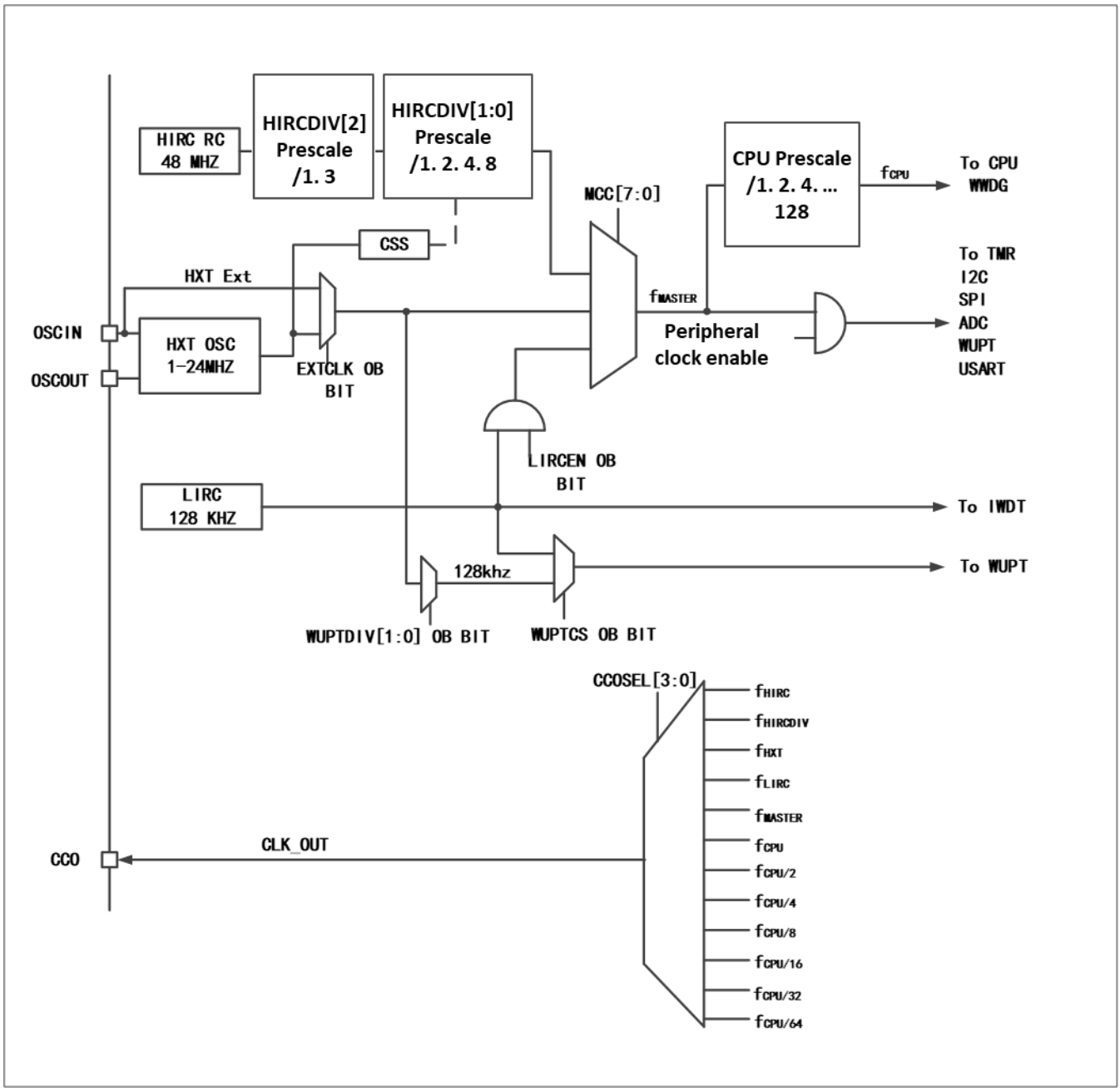
5. System block diagram

Figure 3 System block diagram of APM32F003x4/x6 series



6. Clock tree

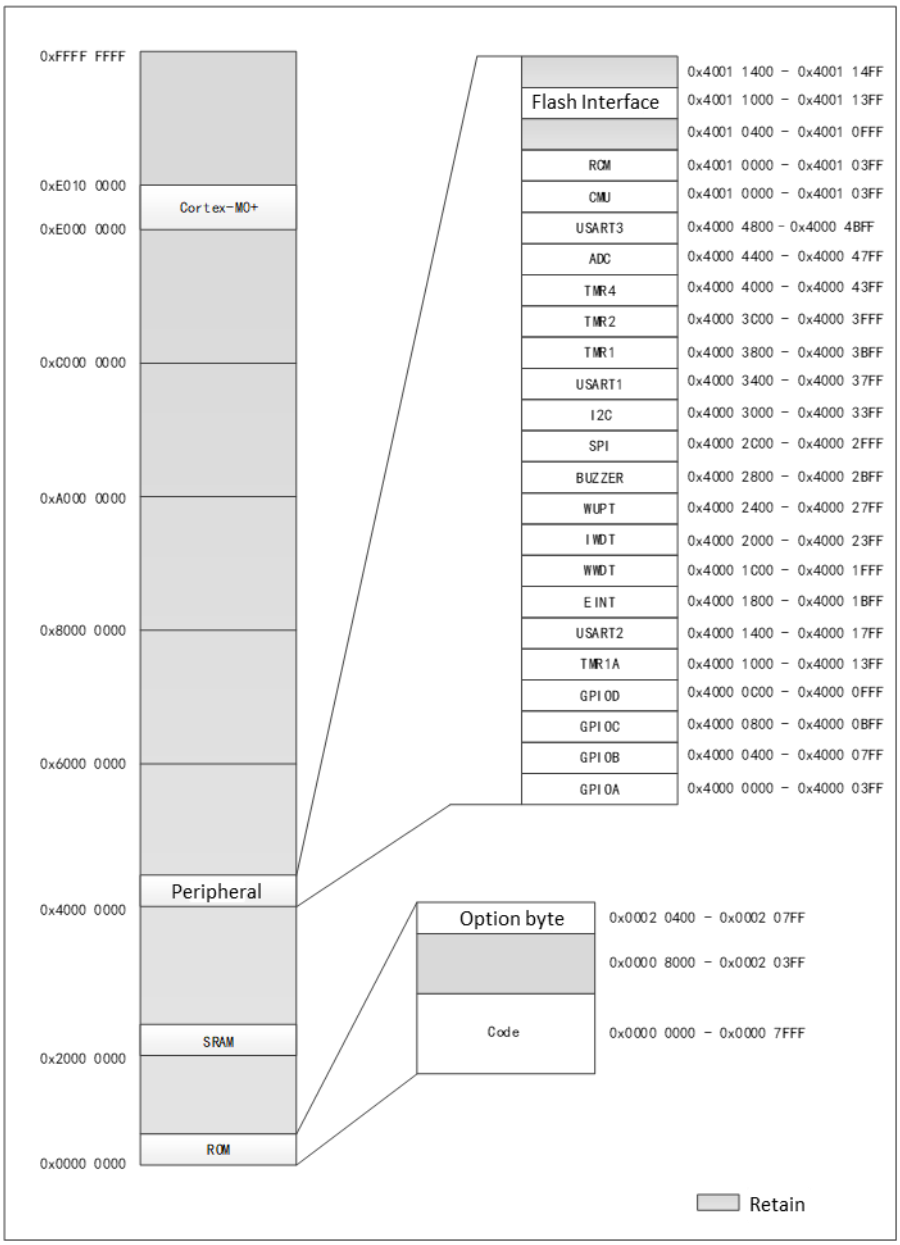
Figure 4 Clock tree of APM32F003x4/x6 series



Note: the counter of WUPT is not provided by f_{MASTER}, so even if the clock of the register has been turned off, the peripheral can continue to run.

7. Address mapping

Figure 5 Address map of APM32F003x4/x6 series



8. Electrical specification

8.1. Test condition

Unless otherwise specified, all voltage parameters are referenced to V_{SS}.

8.1.1. Maximum and minimum value

Unless otherwise specified, all products are tested on the production line at ta = 25 C. Its maximum and minimum values can support the worst environmental

temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line; On the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

8.1.2. Typical value

Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=3.3V and 5V.

8.1.3. Typical curve

Unless otherwise specified, typical curves are only used for design guidance.

8.1.4. Load capacitance

Figure 6 Load conditions when measuring pin parameters

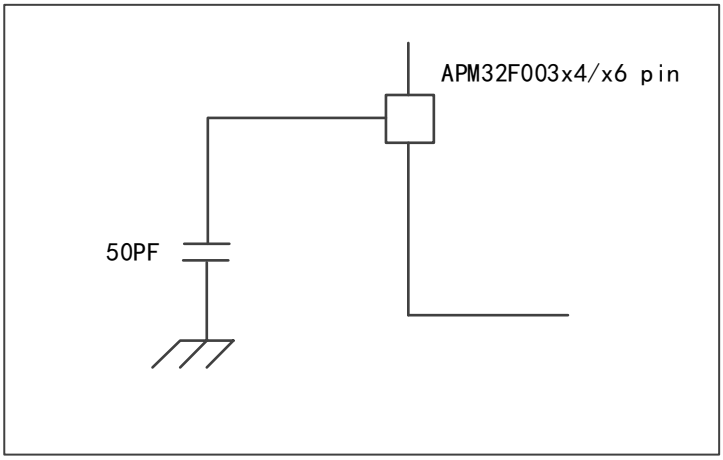
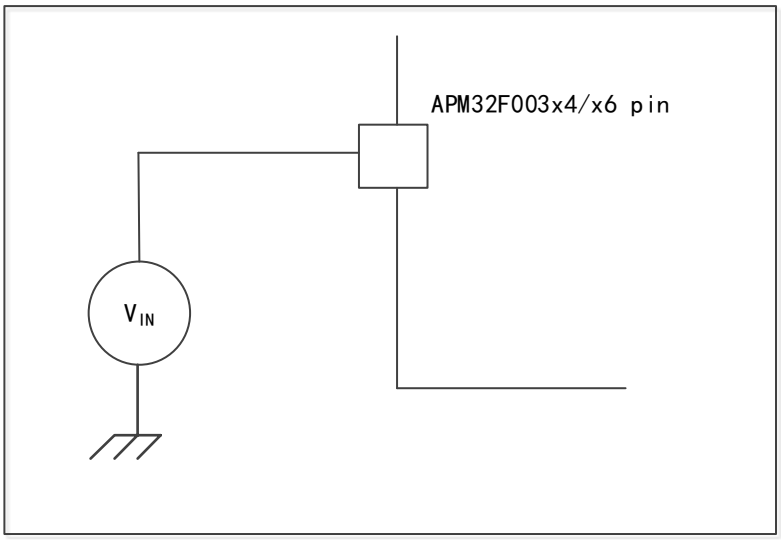


Figure 7 Pin input voltage measurement scheme



8.2. Absolute maximum rating

If the load on the device exceeds the absolute maximum rating, it will cause permanent damage to the device. Only the maximum load that can be borne is given here, and there is no guarantee that the device functions normally under this condition.

8.2.1. Maximum rated voltage characteristics

Table 15 Maximum rated voltage characteristics

Symbol	description	Minimum value	Maximum value	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	0.3	-	V
V_{IN}	Input voltage on the true open drain pin	V_{SS}-0.3	6.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	
$\|V_{DDx}$-$V_{DD}\|$	Voltage difference between different power supply pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Voltage difference between different grounding pins	-	50	

8.2.2. Maximum rated current characteristics

Table 16 Maximum rated current characteristics

Symbol	description	Maximum value	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current)	100	mA
I_{VSS}	Total current through V_{SS} ground (outflow current)	80	
I_{IO}	Current sink on any I/O and control pins	20	
	Pull current on any I/O and control pins	-20	
$I_{INJ(PIN)}$	Injection current of NRST pin	±4	
	Injection current of OSC_IN pin of HXT and OSC_IN pin of LXT	±4	
	Injection current of other pins	±4	
$\Sigma I_{INJ(PIN)}$	Total injection current on all I/O and control pins	±20	

8.2.3. Maximum temperature characteristics

Table 17 Temperature characteristics

Symbol	description	Numerical value	Unit
T_{STG}	Storage temperature range	-65 ~150	°C
T_J	Maximum junction temperature	150	°C

8.2.4. Maximum electrostatic characteristics

Table 18 Electrostatic discharge (ESD) (1)

Symbol	Parameter	Condition	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (manikin)	T_A=+25°C	8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=+25°C	2000	

Note:

1. Samples are measured by a third-party testing organization and are not tested in production.

8.2.5. Static latch

Table 19 Static latch

Symbol	Parameter	Condition	Type
LU	Static latch class	T_A=+25°C/105°C	A

8.3. Testing under general working conditions

Table 20 General working conditions

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz
V_{DD}	Standard operating voltage	-	2.0	5.5	V
V_{CAP}	V_{CORE} external capacitance	-	470	3300	nF

8.3.1. Power-on/power-down reset characteristic test

Table 21 Power-on/power-down reset working conditions (T_A=25℃)

Symbol	Parameter	Condition	Minimu	Typical	Maximu	Unit
t_{TEMP}	Reset release delay	V_{DD} rising	0.58	0.79	0.92	mS
V_{IT+}	Power-on reset threshold	-	1.79	1.83	1.86	V
V_{IT-}	Power failure reset threshold	-	1.70	1.73	1.76	V
$V_{HYS(BOR)}$	BOR hysteresis	-	-	100	-	mV

8.3.2. Power consumption

The current consumption of MCU is affected by many parameters, such as voltage, temperature, IO status, program location in memory, software configuration, frequency and so on. The current values given in this section are measured by executing CRC algorithm, compiling environment Keil V5 and compiling optimization level L0.

The microcontroller is under the following conditions:

- All I/O pins are in input mode and connected to a static level V_{DD} orV_{SS} (non-loaded).
- Unless otherwise specified, all peripherals are turned off.
- Unless otherwise specified, typical values are measured at 25℃, 3.3V or 5V.
- Unless otherwise specified, the maximum values are measured at 105℃ and 5.5V power supply.

Table 22 Typical operating mode power consumption

Symbol	Parameter	Condition	Voltage (TA=25℃)		Unit
			3.3V	5V	
I_{DD}	Supply current in running mode in RAM	HXT=24MHz，F_{CPU}=24MHZ	2.5	3.1	mA
		HXT=16MHz，F_{CPU}=16MHZ	2	2.6	
		HIRC=48MHz，F_{CPU}=48MHZ	3.2	3.2	
		HIRC=48MHz，F_{CPU}=24MHZ	2.2	2.2	
		HIRC=48MHz，F_{CPU}=375kHZ	0.94	0.96	
		HIRC=48MHz，F_{CPU}=46.875kHZ	0.51	0.51	
		HIRC=16MHZ，F_{CPU}=16MHZ	1.4	1.4	
		HIRC=16MHZ，F_{CPU}=125kHZ	0.61	0.61	
		HIRC=16MHZ，F_{CPU}=15.625MHZ	0.47	0.47	
		LIRC=128KHZ，F_{CPU}=128KHZ	0.33	0.34	
	Supply current in running mode in Flash	HXT=24MHz，F_{CPU}=24MHZ	4.2	4.7	
		HXT=16MHz，F_{CPU}=16MHZ	3.1	3.7	
		HIRC=48MHz，F_{CPU}=48MHZ	4.8	4.8	
		HIRC=48MHz，F_{CPU}=24MHZ	3.8	3.8	
		HIRC=48MHz，F_{CPU}=375kHZ	0.97	0.97	
		HIRC=48MHz，F_{CPU}=46.875kHZ	0.51	0.52	

		HIRC=16MHZ，F_{CPU}=16MHZ	2.5	2.6	
		HIRC=16MHZ，F_{CPU}=125kHZ	0.62	0.63	
		HIRC=16MHZ，F_{CPU}=15.625kHZ	0.47	0.47	
		LIRC=128KHZ，F_{CPU}=128KHZ	0.34	0.34	

Table 23 Maximum power consumption in operation mode

Symbol	Parameter	Condition	Voltage (TA=105℃)			Unit
			3.3V	5V	5.5V	
I_{DD}	Supply current in running mode in RAM	HXT=24MHz，F_{CPU}=24MHZ	2.68	3.30	3.56	mA
		HXT=16MHz，F_{CPU}=16MHZ	2.14	2.75	2.99	
		HIRC=48MHz，F_{CPU}=48MHZ	3.63	3.70	3.75	
		HIRC=48MHz，F_{CPU}=24MHZ	2.42	2.47	2.54	
		HIRC=48MHz，F_{CPU}=375kHZ	1.11	1.13	1.22	
		HIRC=48MHz，F_{CPU}=46.875kHZ	0.63	0.64	0.74	
		HIRC=16MHZ，F_{CPU}=16MHZ	1.57	1.58	1.68	
		HIRC=16MHZ，F_{CPU}=125kHZ	0.73	0.74	0.84	
		HIRC=16MHZ，F_{CPU}=15.625MHZ	0.58	0.58	0.68	
		LIRC=128KHZ，F_{CPU}=128KHZ	0.43	0.43	0.55	
	Supply current in running mode in Flash	HXT=24MHz，F_{CPU}=24MHZ	4.61	5.30	5.49	
		HXT=16MHz，F_{CPU}=16MHZ	3.42	4.10	4.30	
		HIRC=48MHz，F_{CPU}=48MHZ	5.47	5.62	5.64	
		HIRC=48MHz，F_{CPU}=24MHZ	4.35	4.47	4.50	
		HIRC=48MHz，F_{CPU}=375kHZ	1.14	1.25	1.28	
		HIRC=48MHz，F_{CPU}=46.875kHZ	0.63	0.73	0.77	
		HIRC=16MHZ，F_{CPU}=16MHZ	2.85	2.86	2.96	
		HIRC=16MHZ，F_{CPU}=125kHZ	0.75	0.75	0.85	
		HIRC=16MHZ，F_{CPU}=15.625kHZ	0.58	0.58	0.68	
		LIRC=128KHZ，F_{CPU}=128KHZ	0.44	0.55	0.58	

Table 24 Typical power consumption in WAIT mode

Symbol	Parameter	Condition	Voltage (TA=25℃)		Unit
			3.3V	5V	
I_{DD}	Supply current in WAIT mode	HXT=24MHz，F_{CPU}=24MHZ	1.5	2.04	mA
		HXT=16MHz，F_{CPU}=16MHZ	1.32	1.9	
		HIRC=48MHz，F_{CPU}=48MHZ	1.2	1.2	
		HIRC=48MHz，F_{CPU}=24MHZ	1.1	1.1	
		HIRC=48MHz，F_{CPU}=375kHZ	0.93	0.93	
		HIRC=48MHz,F_{CPU}=46.875kHZ	0.51	0.51	
		HIRC=16MHZ，F_{CPU}=16MHZ	0.68	0.69	
		HIRC=16MHZ，F_{CPU}=125kHZ	0.60	0.61	
		HIRC=16MHZ,F_{CPU}=15.625MHZ	0.46	0.47	
		LIRC=128KHZ，F_{CPU}=128KHZ	0.33	0.33	

Table 25 Maximum power consumption in WAIT mode

Symbol	Parameter	Condition	Voltage (TA=105℃))			Unit
			3.3V	5V	5.5V	
I_{DD}	Supply current in WAIT mode	HXT=24MHz，F_{CPU}=24MHZ	1.55	2.10	2.40	mA
		HXT=16MHz，F_{CPU}=16MHZ	1.39	1.95	2.21	
		HIRC=48MHz，F_{CPU}=48MHZ	1.36	1.36	1.45	
		HIRC=48MHz，F_{CPU}=24MHZ	1.27	1.27	1.37	
		HIRC=48MHz，F_{CPU}=375kHZ	1.09	1.09	1.18	
		HIRC=48MHz,F_{CPU}=46.875kHZ	0.62	0.63	0.71	
		HIRC=16MHZ，F_{CPU}=16MHZ	0.82	0.83	0.90	
		HIRC=16MHZ，F_{CPU}=125kHZ	0.73	0.73	0.86	
		HIRC=16MHZ,F_{CPU}=15.625MHZ	0.58	0.58	0.71	
		LIRC=128KHZ，F_{CPU}=128KHZ	0.43	0.43	0.51	

Table 26 Typical power consumption in active halt mode

Symbol	Parameter	Condition			Voltage (TA=25℃)		Unit
		MVR	Flash mode	**Clock source**	**3.3V**	**5V**	
I_{DD}	Supply current in active shutdown mode	Turn on	Operation	HXT=16MHZ	780	1360	μA
		Turn on	Operation	HXT=24MHZ	800	1390	
		Turn on	Power down	HXT=16MHZ	780	1360	
		Turn on	Power down	HXT=24MHZ	800	1390	
		Turn on	Operation	LIRC=128KHZ	17.1	18.8	
		Turn on	Power down	LIRC=128KHZ	17.0	18.5	
		Turn off	Operation	LIRC=128KHZ	4.9	6.6	
		Turn off	Power down	LIRC=128KHZ	4.8	6.4	

Table 27 Maximum power consumption in active halt mode

Symbol	Parameter	Condition			Voltage (TA=105℃))			Unit
		MVR	**Flash mode**	**Clock source**	3.3V	5V	5.5V	
I_{DD}	Supply current in active shutdown mode	Turn on	Operation	HXT=16MHZ	780	1350	1640	μA
		Turn on	Operation	HXT=24MHZ	810	1380	1670	
		Turn on	Power down	HXT=16MHZ	780	1350	1630	
		Turn on	Power down	HXT=24MHZ	800	1380	1670	
		Turn on	Operation	LIRC=128KHZ	55.64	57.72	59.82	
		Turn on	Power down	LIRC=128KHZ	48.24	50.98	52.42	

		Turn off	Operation	LIRC=128KHZ	32.30	34.34	35.34	
		Turn off	Power down	LIRC=128KHZ	26.44	28.53	29.46	

Table 28 Typical power consumption in halt mode

Symbol	Parameter	Condition	Voltage (TA=25℃)		Unit
			3.3V	5V	
I_{DD}	Supply current in halt mode	Running mode of Flash, HIRC as clock source after wake up	3.53	5.2	μA
		Flash power-down mode, HIRC as clock source after wake up	3.43	5.0	

Table 29 Maximum power consumption in shutdown mode

Symbol	Parameter	Condition	Voltage (TA=105℃))			Unit
			3.3V	5V	5.5V	
I_{DD}	Supply current in halt mode	Running mode of Flash, HIRC as clock source after wake up	30.65	32.39	33.77	μA
		Flash power-down mode, HIRC as clock source after wake up	24.70	26.72	27.44	

Table 30 Typical value of peripheral power consumption (V_{DD}=5V,T_A=25℃)

Symbol	Parameter	16Mhz	48Mhz	Unit
I_{DD}(TMR1)	TMR1 supply current	98	300	μA
I_{DD}(TMR1A)	TMR1A supply current	58	170	
I_{DD}(TMR2)	TMR2 supply current	56	168	
I_{DD}(TMR4)	TMR4 timer supply current	15	46	
I_{DD}(USART1)	USART1 supply current	56	168	
I_{DD}(USART2)	USART2 supply current	100	310	
I_{DD}(USART3)	USART3 supply current	55	170	

I_{DD}(SPI)	SPI supply current	23	68	
I_{DD}(I2C)	I2C supply current	37	110	
I_{DD}(ADC1)	Supply current during ADC1 conversion	290	680	

8.3.3. External clock source characteristics

High Speed External Clock Generated by Crystal Resonator (HXT osc)

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 31 Characteristics of HXT 1-48MHz oscillator

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HXT}	Oscillator frequency	-	1	-	48	MHz
R_F	Feedback resistance	-	-	300	-	kΩ
C	Recommended load capacitance	-	-	-	20	pF
$I_{DD(HXT)}$	HXT oscillator power consumption	C=20pF, f_{OSC}=16MHz	-	-	6 (startup) 1.6 (stabilized)	mA
		C=10pF, f_{OSC}=16MHz	-	-	6 (startup) 1.2 (stabilized)	
$t_{SU(HXT)}$	Startup time	V_{DD} is stable	-	1	-	ms

8.3.4. Internal clock source characteristics

Test of High Speed Internal (HIRC) Oscillator

Table 32 HIRC oscillator characteristics

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
f_{HIRC}	Frequency	-		-	48	-	MHz
ACC_{HIRC}	Accuracy of HIRC oscillator	User calibration	Given V_{DD} and T_A, the user uses the CLK_HIRCTRIMR register for calibration.	-1	-	1	%
		Factory calibration	V_{DD}=3.3-5V, -40°C≤T_A≤105°C	-5	-	5	%
$t_{SU(HIRC)}$	HIRC oscillator start-up time (including calibration)	-		-	-	0.8	μs
$I_{DD(HIRC)}$	HIRC oscillator power consumption	-		-	120		μA

Low speed internal (LIRC) oscillator test

Table 33 LIRC oscillator characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LIRC}	Frequency	-	128	-	KHz
ACC_{LIRC}	Accuracy of oscillator (V_{DD}=3.3-5V,-40°C≤T_A≤105°C)	-5	-	5	%

$t_{SU(LIRC)}$	Startup time of LIRC oscillator	-	-	5	μs
$I_{DD(LIRC)}$	LIRC oscillator power consumption	-	5	-	μA

Time to wake up from low power mode

HIRC is used as the clock source for wake-up.

Table 34 Wake-up time in low power mode

Symbol	Parameter	Condition			Typical value	Maximum value	Unit
$t_{WU(WFI)}$	Wake-up time from waiting to running	$f_{CPU}=f_{MASTER}$=48MHz			0.61	-	us
		$f_{CPU}=f_{MASTER}$=24MHz			1.17	-	
		$f_{CPU}=f_{MASTER}$=12MHz			2.36	-	
		$f_{CPU}=f_{MASTER}$=6MHz			4.67	-	
$t_{WU(AH)}$	Wake-up time from active shutdown mode to run mode	MVR on	Flash running	HIRC after wake-up	5.52	8.36	
		MVR off	Flash running	HIRC after wake-up	53.13	55	
$t_{WU(H)}$	Wake-up time from shutdown to operation	Flash running mode			55.21	-	

8.3.5. Flash memory characteristics

Table 35 Flash storage characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16-bit programming	T_A=-40~105°C V_{DD}=2.95~5.0V	22.4	22.97	23.8	μs

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
	time					
t_{ERASE}	Page (1kbyte) erase time	T_A=-40~105°C V_{DD}=2.95~5.0V	1.48	1.55	1.64	ms
t_{ME}	Whole erase time	T_A=25°C V_{DD}=3.3V	6.32	6.57	6.96	ms
t_{RET}	Data saving time	T_A=55℃	20	-	-	years
N_{RW}	Erase cycle	T_A=25°C	10K	-	-	cycles
V_{prog}	Programming voltage	T_A=-40~105°C	2	-	5.5	V

8.3.6. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 36 NRST pin characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$	NRST input low voltage	-	-0.3V	-	0.3xV_{DD}	V
$V_{IH(NRST)}$	NRST input high voltage	-	0.7xV_{DD}	-	V_{DD}+0.3	
$V_{OL(NRST)}$	NRST outputs a low voltage	IOL=2mA	-	-	0.5	V
$V_{hys(NRST)}$	NRST Schmitt trigger Voltage hysteresis	-	-	600	-	mV
R_{PU}	pull up resistor	-	30	60	80	kΩ
$V_{F(NRST)}$	NRST input filter pulse	-	-	-	75	ns
$V_{NF(NRST)}$	NRST input unfiltered pulse	-	500	-	-	ns
$t_{OP(NRST)}$	Output pulse width of	-	20	-	-	us

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
	NRST					

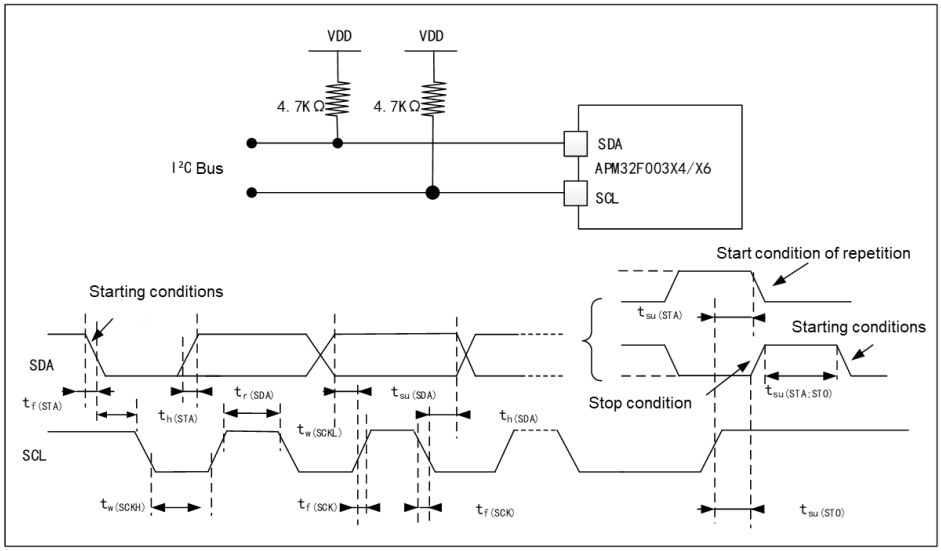
8.3.7. communication interface

I2C interface characteristics

Table 37 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	5.03	-	1.73	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.90	-	0.72	-	
$t_{su(SDA)}$	SDA setup time	4420	-	1120	-	ns
$t_{h(SDA)}$	SDA data holding time	0	313.09	0	335.97	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	300.12	-	301.24	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	21.3	-	21.51	
$t_{h(STA)}$	Start condition holding time	4.98	-	0.82	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.95	-	0.87	-	
$t_{su(STO)}$	Setup time of stop condition	4.94	-	0.84	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	5.4	-	2.08	-	μs

Figure 8 Bus AC waveform and test circuit



SPI interface characteristics

Table 38 SPI characteristics

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	holotype		8	MHz
		Slave mode		8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C=30pF	-	16.854	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	433.33	-	
$t_{h(NSS)}$	NSS holding time	Slave mode	115.43	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	holotype	54.592	57.4723	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	holotype	30.304	-	
		Slave mode	50.889	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input holding time	holotype	64.746	-	
		Slave mode	52.22	-	
$t_{a(SO)}$	Data output access time	Slave mode	2.530	12.272	
$t_{dis(SO)}$	Data output prohibition time	Slave mode	25.235	-	
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	29.605	

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	7.220	
$t_{h(SO)}$	Data output holding time	Slave mode (after enable edge)	16.222	-	
$t_{h(MO)}$		Master mode (after enable edge)	8.356	-	

Figure 9 SPI timing diagram—slave mode and CPHA=0

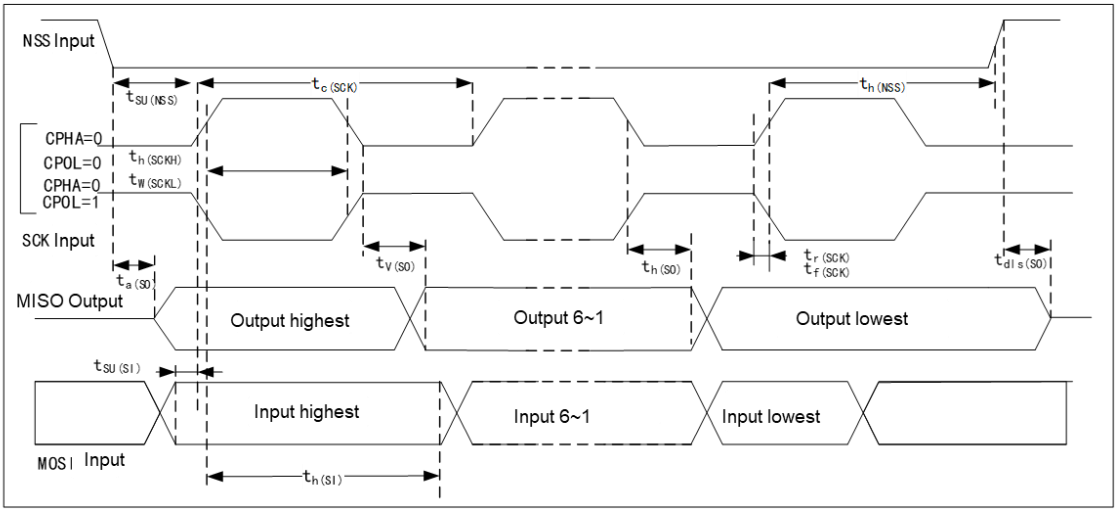
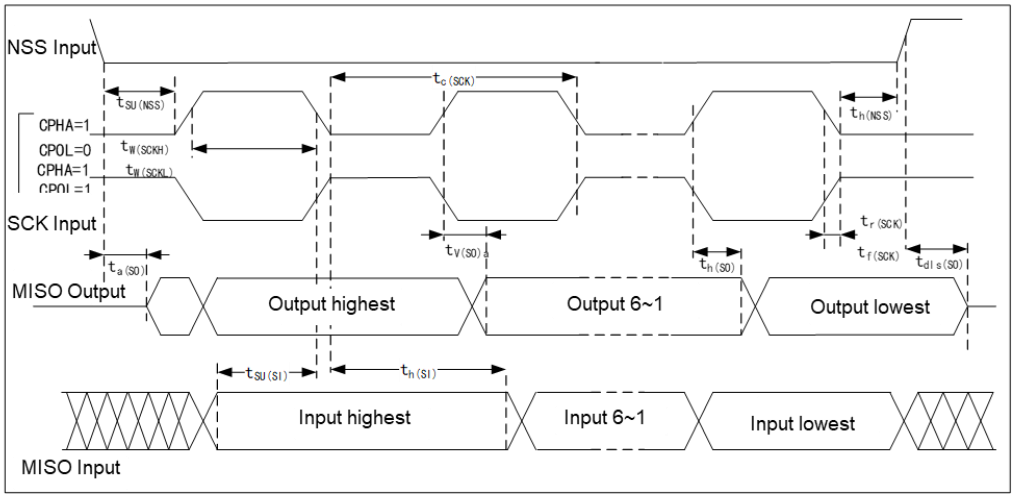


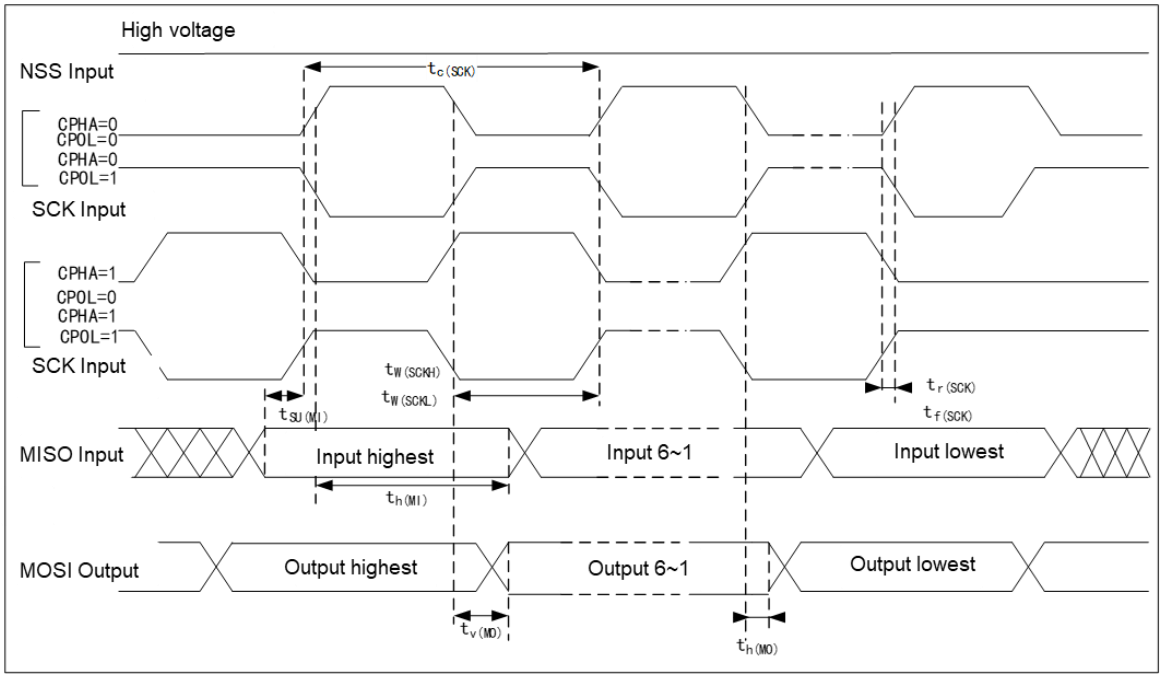
Figure 10 SPI timing diagram—slave mode and CPHA=1(1)



Note:

（1） The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 11 SPI timing diagram-main mode (1)



Note:

(1) the measuring points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

8.3.8. ADC characteristics

Table 39 12-bit ADC features

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Service voltage	-	2.4	-	5.5	V
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	-	5	pF
R_{ADC}	Sampling resistance	-	-	-	1000	ohm
t_S	Sampling time	f_{ADC}=14MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion Time	f_{ADC}=14MHz	1	-	18	μs

Table 40 12-bit ADC accuracy

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
$\|E_T\|$	Total uncorrected error	3.3V~5V	6.5	-	LSB
$\|E_O\|$	offset error	3.3V~5V	2	-	
$\|E_G\|$	Gain error	3.3V~5V	4.5	-	
$\|E_D\|$	Differential linear error	3.3V~5V	1.5	-	
$\|E_L\|$	Integral linearity error	3.3V~5V	2.8	-	

8.3.9. I/O port characteristics

Table 41 I/O static characteristics and AC characteristics (V_{DD}=2.0~5.5V, T_A=-40~105°C)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Input low level voltage	V_{DD}=5V	-0.3		0.3xV_{DD}	V
V_{IH}	Input high level voltage		0.7xV_{DD}		V_{DD}+0.3	
V_{hys}	Voltage hysteresis			700		mV
Rpu	pull up resistor	V_{DD}=5V,V_{IN}=V_{SS}	55	63	66	kΩ
t_R,t_F	Rise and fall time (10%-90%)	Fast I/O port with load capacitance of 50pF			17	nS
		Standard and high sinkI/O port, load capacitance 50pF			17	
I_{lkg}	Digital input leakage current	V_{SS}≤V_{IN}≤V_{DD}			±1	μA

Table 42 Output drive current (true open drain port)

Symbol	Parameter	Condition	Maximum value	Unit
V_{OL}	Output low level	I_{IO}=10mA，V_{DD}=5.0V	0.8	V
	Output low level	I_{IO}=10mA，V_{DD}=3.3V	0.7	
	Output low level	I_{IO}=20mA，V_{DD}=5.0V	1.2	V

Table 43 Output drive current (high sink current port)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL}	Output low level	I_{IO}=10mA，V_{DD}=5.0V	-	0.4	
	Output low level	I_{IO}=10mA，V_{DD}=3.3V	-	0.6	V
	Output low level	I_{IO}=20mA，V_{DD}=5.0V	-	0.9	
V_{OH}	Output high level	I_{IO}=10mA，V_{DD}=5.0V	4.4	-	V

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
	Output high level	I_{IO}=10mA，V_{DD}=3.3V	2.5	-	
	Output high level	I_{IO}=20mA，V_{DD}=5.0V	3.8	-	

9. Package characteristics

Table 44 APM32F003x4/x6

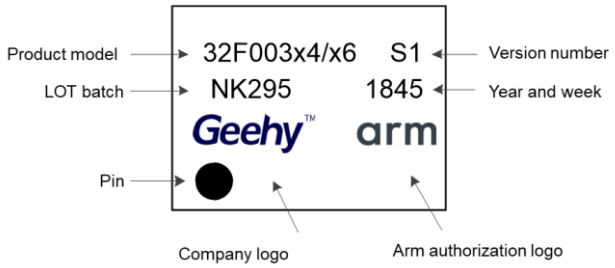
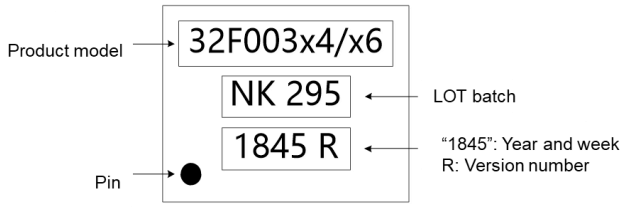
Package Name	Size	Marking of Apex samples
TSSOP20、SOP20	6.5*4.4*0.9	
QFN20	3*3*0.55	

Figure 12 Package diagram of TSS0P20

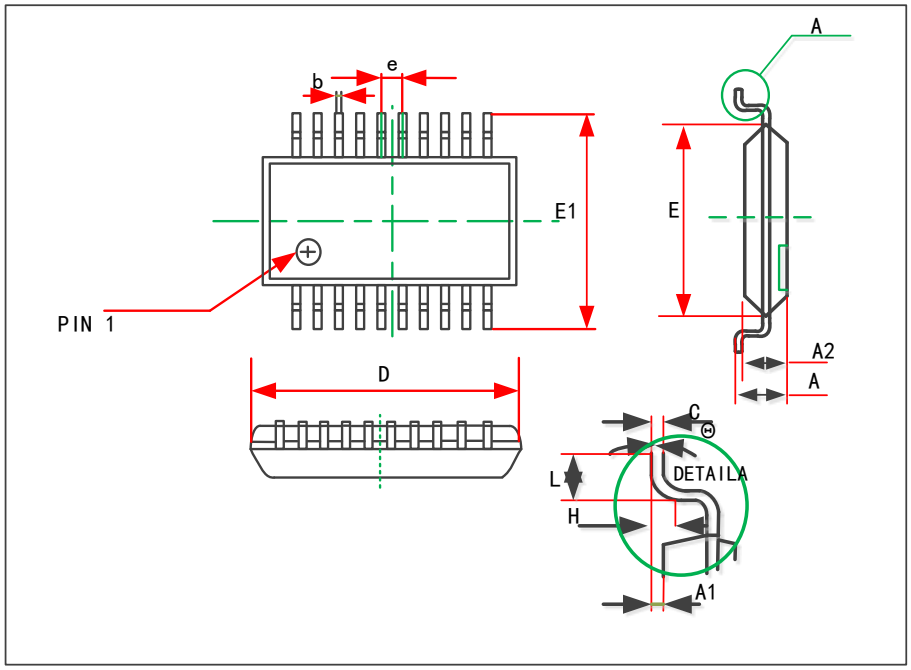

b
e
E1
PIN 1
D
A
E
A2
A
C
DETAILA
L
H
A1

Table 45 Package dimensions of TSS0P20

SYMBOL	Dimensions IN Millimeters		Dimensions IN Inches	
	MIN	MAX	MIN	MAX
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	-	1.200	-	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Figure 13 Package diagram of SOP20

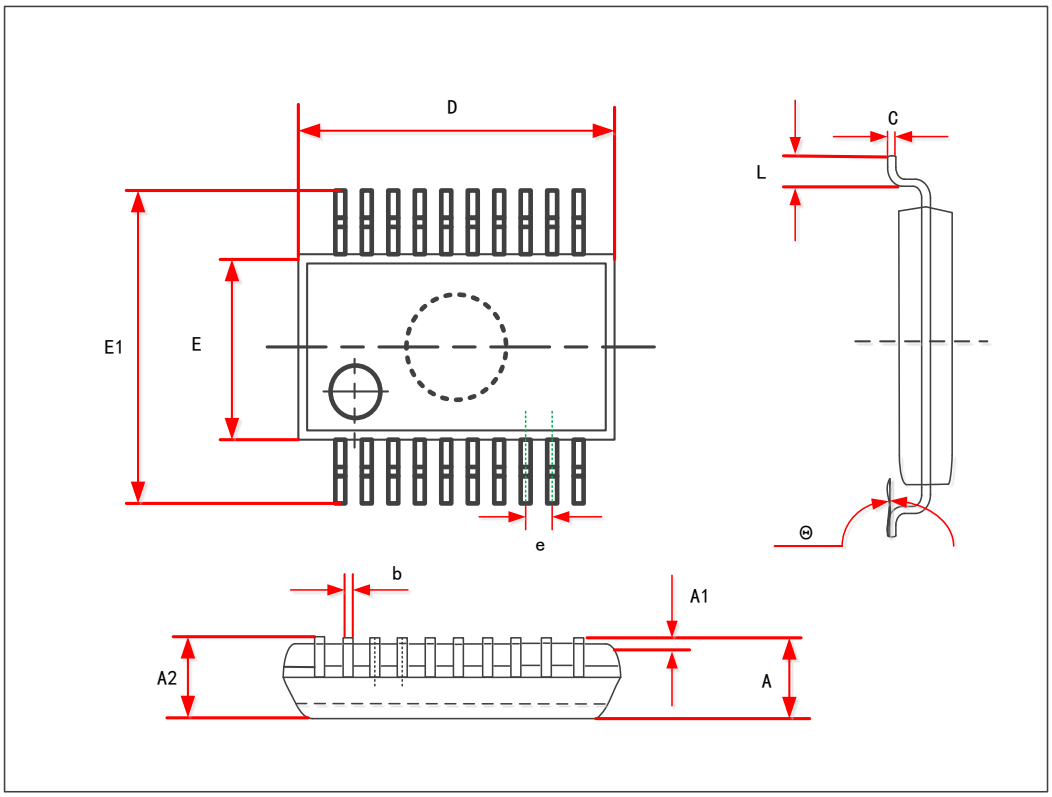


Table 46 Package dimensions of SOP20

SYMBOL	Dimensions IN Millimeters		Dimensions IN Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°		8°

Figure 14 Package diagram of QFN20

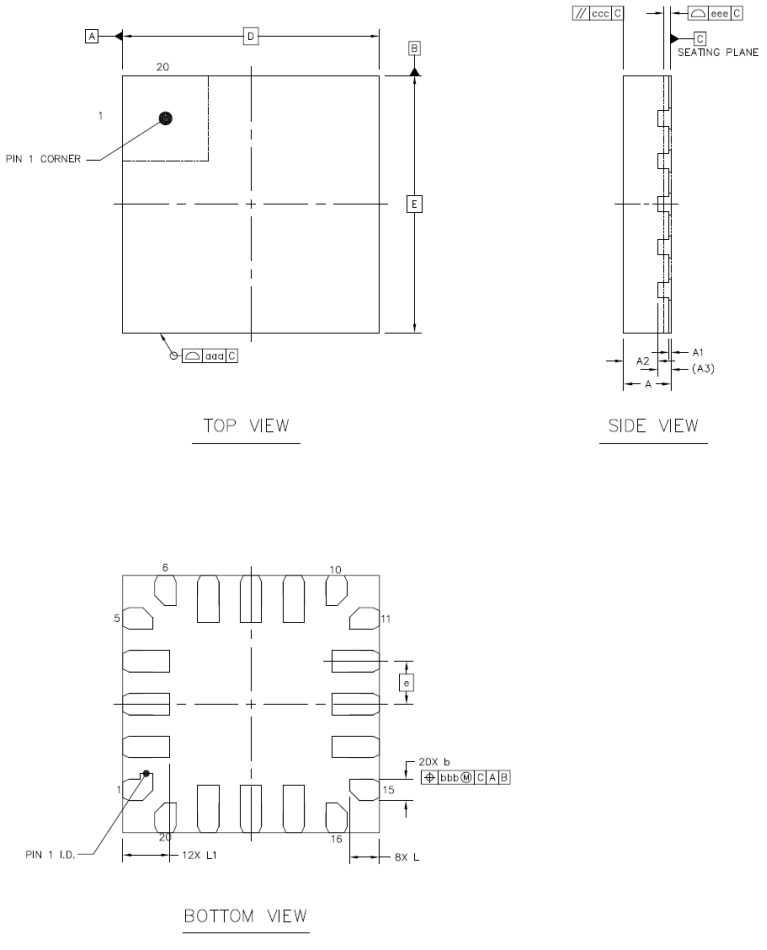


Table 47 Package dimensions of QFN20

-		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THIXKNESS		A2	-	0.4	-
L/F THICKNESS		A3	0.152REF		
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	3 BSC		
	Y	E	3 BSC		
LEAD PITCH		e	0.5 BSC		
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.45	0.55	0.65
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANAPITY		eee	0.08		
LEAD OFFSET		bbb	0.1		

10. Ordering information

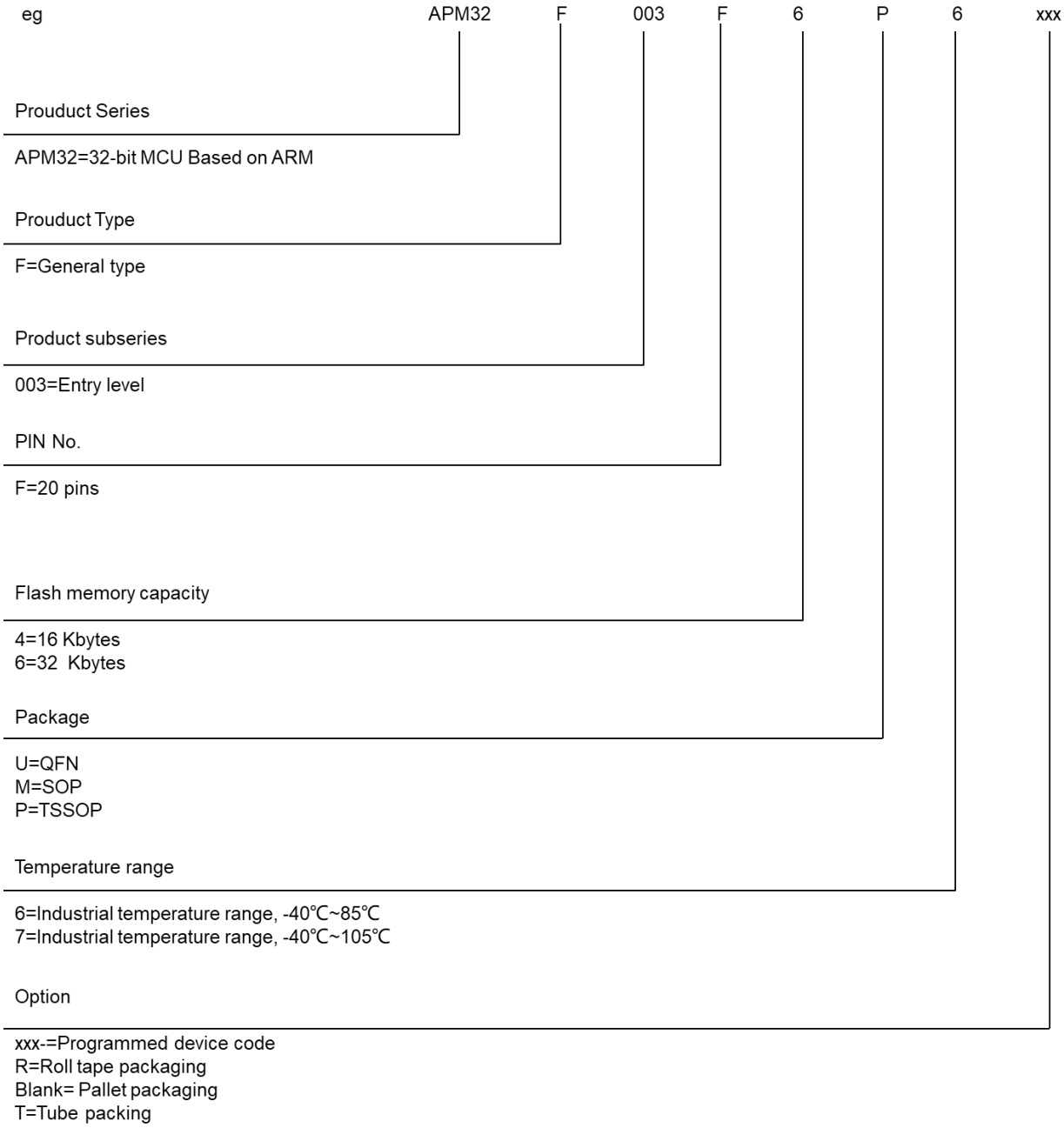


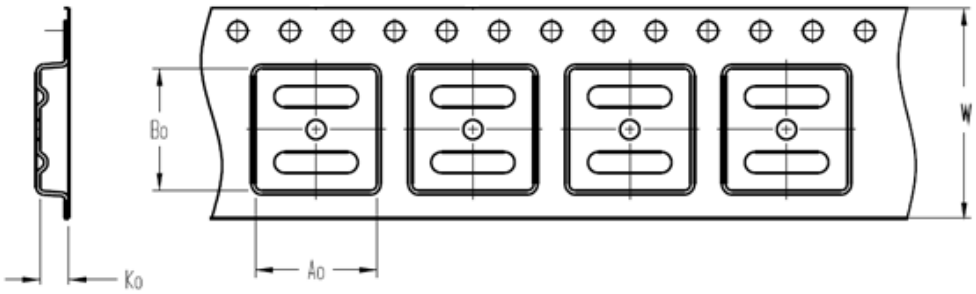
Table 48 Order information list

Order code	Flash(KB)	SRAM(KB)	Packaging	SPQ	Temperature range
APM32F003F4P6-T	16	2	TSSOP20	14720	Industrial grade -40℃~85℃
APM32F003F6P6-T	32	4	TSSOP20	14720	Industrial grade

Order code	Flash(KB)	SRAM(KB)	Packaging	SPQ	Temperature range
					-40℃~85℃
APM32F003F4U6-R	16	2	QFN20	5000	Industrial grade -40℃~85℃
APM32F003F4U6	16	2	QFN20	6240	Industrial grade -40℃~85℃
APM32F003F6U6-R	32	4	QFN20	5000	Industrial grade -40℃~85℃
APM32F003F6U6	32	4	QFN20	6240	Industrial grade -40℃~85℃
APM32F003F4M6-T	16	2	SOP20	11200	Industrial grade -40℃~85℃
APM32F003F6M6-T	32	4	SOP20	11200	Industrial grade -40℃~85℃

11. Packaging information

Figure 15 Tape Dimensions



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Figure 16 Quadrant allocation in PIN1 direction in tape

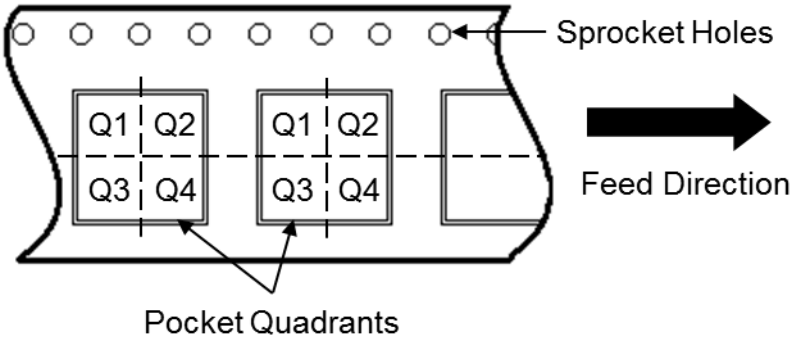


Figure 17 Reel Dimensions

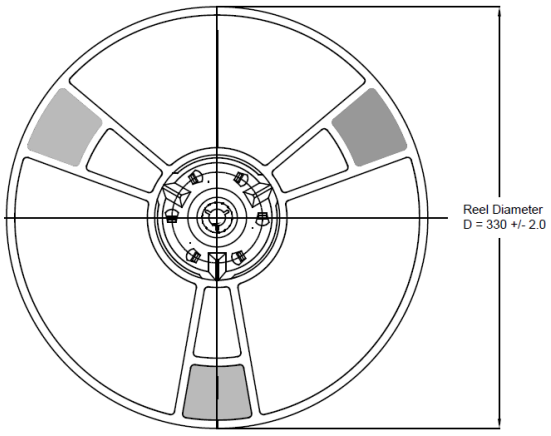


Table 49 Tape packaging parameter specification table

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32F003F6U6	QFN	20	5000	330	3.3	3.3	0.8	12	Q1
APM32F003F4U6	QFN	20	5000	330	3.3	3.3	0.8	12	Q1

Figure 18 Pin1 Orientation and tray chamfer

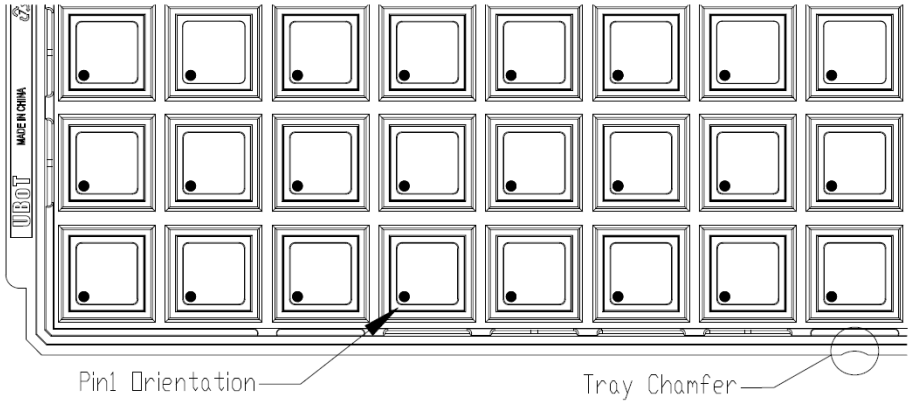


Figure 19 Tray Dimensions

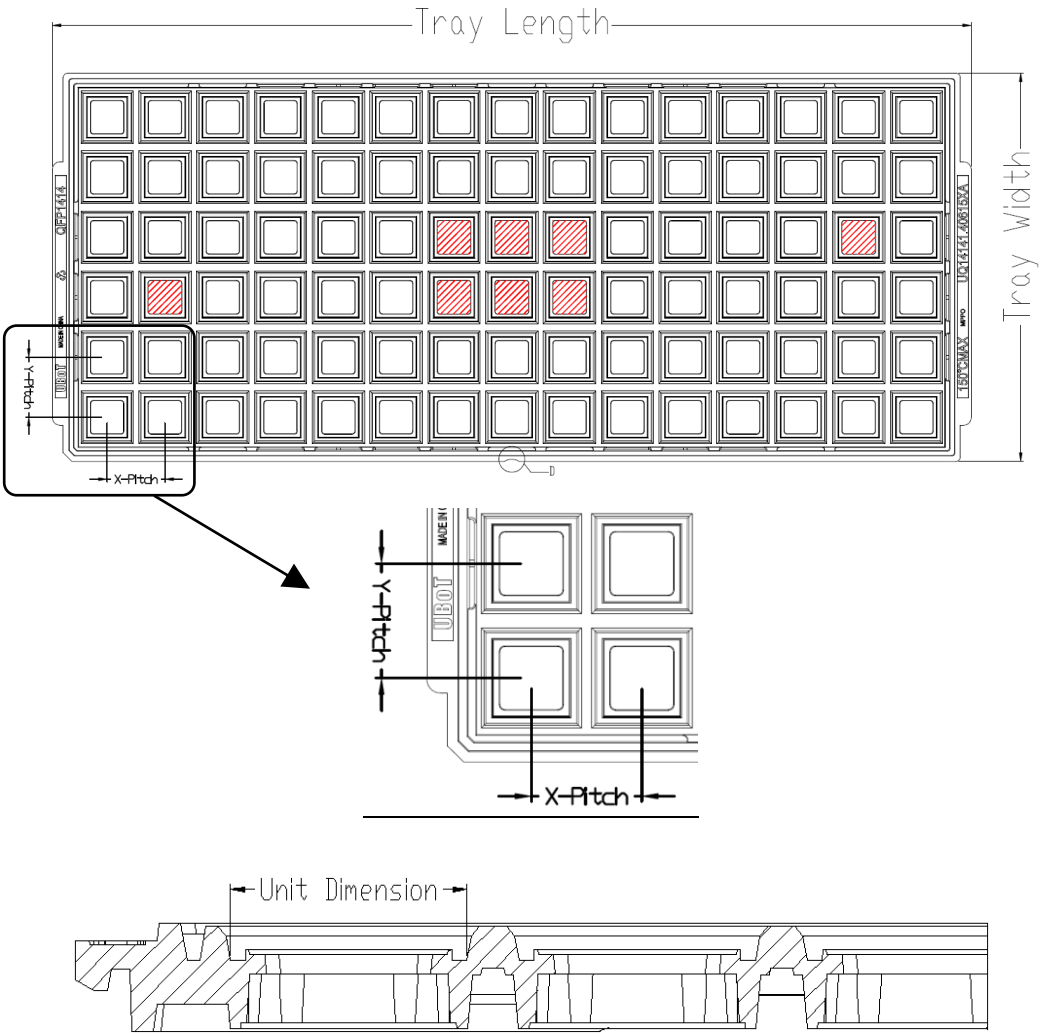


Table 50 Tray packaging parameter specification table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32F003F6U6	QFN	20	6240	3.2	3.2	7.5	7.5	322.6	135.9
APM32F003F4U6	QFN	20	6240	3.2	3.2	7.5	7.5	322.6	135.9

Figure 20 Package drawing of SOP&TSSOP material pipe

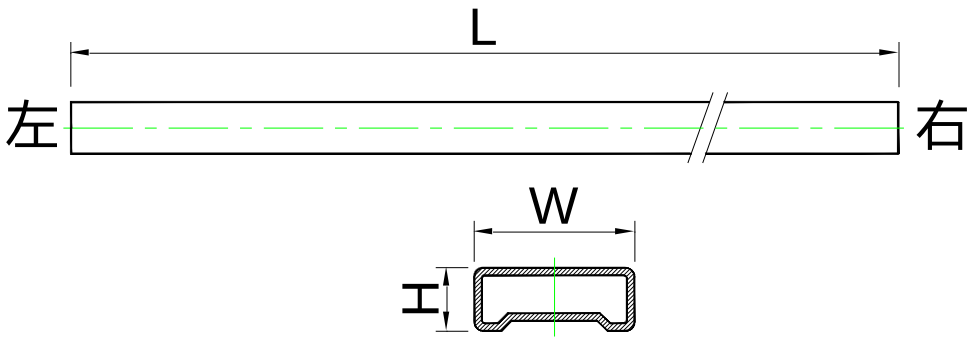


Table 51 Specification table of SOP&TSSOP material tube packaging parameters

Device	Package Type	Pins	Qty Per Tube	SPQ	L (mm)	W (mm)	H (mm)
APM32F003F6P6	TSSOP20	20	46	14720	327	8.5	3.2
APM32F003F4P6	TSSOP20	20	46	14720	327	8.5	3.2
APM32F003F6M6	SOP20	20	35	11200	516	12.7	5
APM32F003F4M6	SOP20	20	35	11200	516	12.7	5

12. Naming of common functional modules

Table 52 Naming of common functional modules

Naming of common functional modules	
Description in Chinese	Abbreviations
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management unit	RCM
External interrupt	EINT
Universal IO	GPIO
Multiplex IO	AFIO
Wake up controller	WAKEUP
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power management unit	PMU
Backup register	BAKR
DMA controller	DMA
Digital analogue converter	ADC
Digital analogue converter	DAC
Real-time clock	RTC
External memory controller	EMMC
SDIO interface	SDIO
USB chip controller	USBD
controller area network	CAN
USB OTG	OTG
Ethernet	ETH
I2C interface	I2C
serial peripheral interface	SPI
Universal asynchronous transceiver	USART
Universal asynchronous synchronous transceiver	USART
Flash interface control unit	FMC

13. version history

Date	Revision	Change
2019.12.27	V1.0.0	New folder
2020.06.19	V1.0.1	Delete P1 information of table 49
2020.07.06	V1.0.2	Modify the cover page and directory format
2020.09.04	V1.1	(1) Modify the error in Table 14 （Pin definition of APM32F003x4/x6(20PIN)）; (2) Adjust the document font; (3) Modify the naming rules in the Ordering Information（Chapter 10）; (4) Modify the order code in Table 48 （Ordering information list）and add a column of minimum number of packages（SPQ）

Table 53 Document revision history