

74ALVC74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 6 — 27 July 2021

Product data sheet

1. General description

The 74ALVC74 is a dual positive edge triggered, D-type flip-flop. It has individual data (nD) inputs, clock (nCP) inputs, set (nSD) and (nRD) inputs, and complementary nQ and nQ outputs.

The set and reset are asynchronous active LOW inputs that operate independently of the clock input. Information on the data input is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse. The nD inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features and benefits

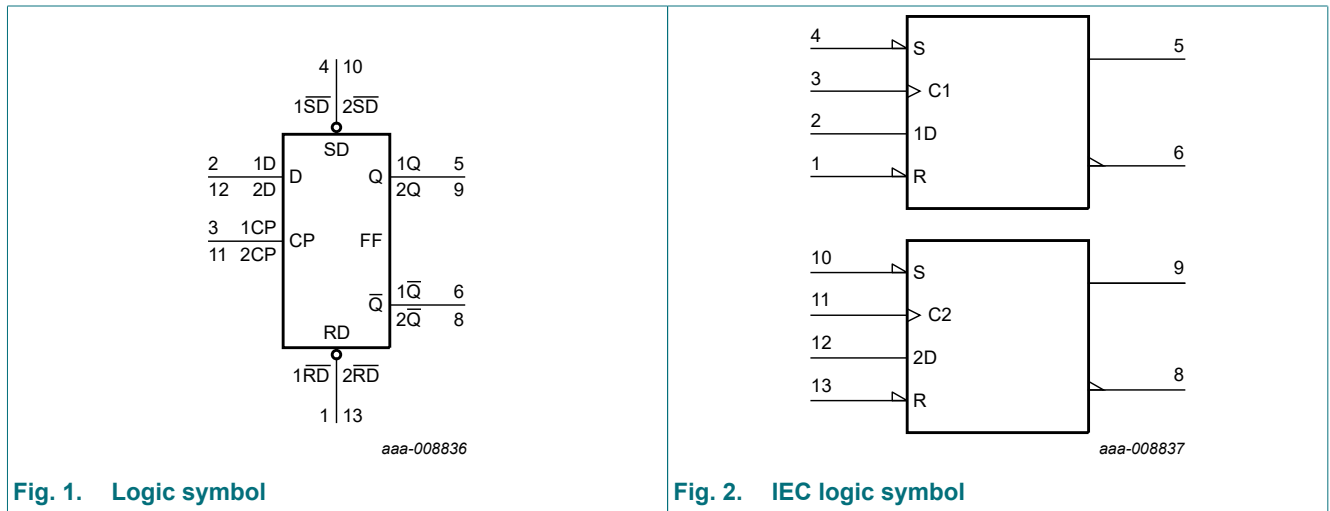
- Wide supply voltage range from 1.65 V to 3.6 V
- Complies with JEDEC standard:
 - JESD8-7 (1.65 to 1.95 V)
 - JESD8-5 (2.3 to 2.7 V)
 - JESD8B (2.7 to 3.6 V)
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC74D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC74PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC74BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram



Dual D-type flip-flop with set and reset; positive-edge trigger

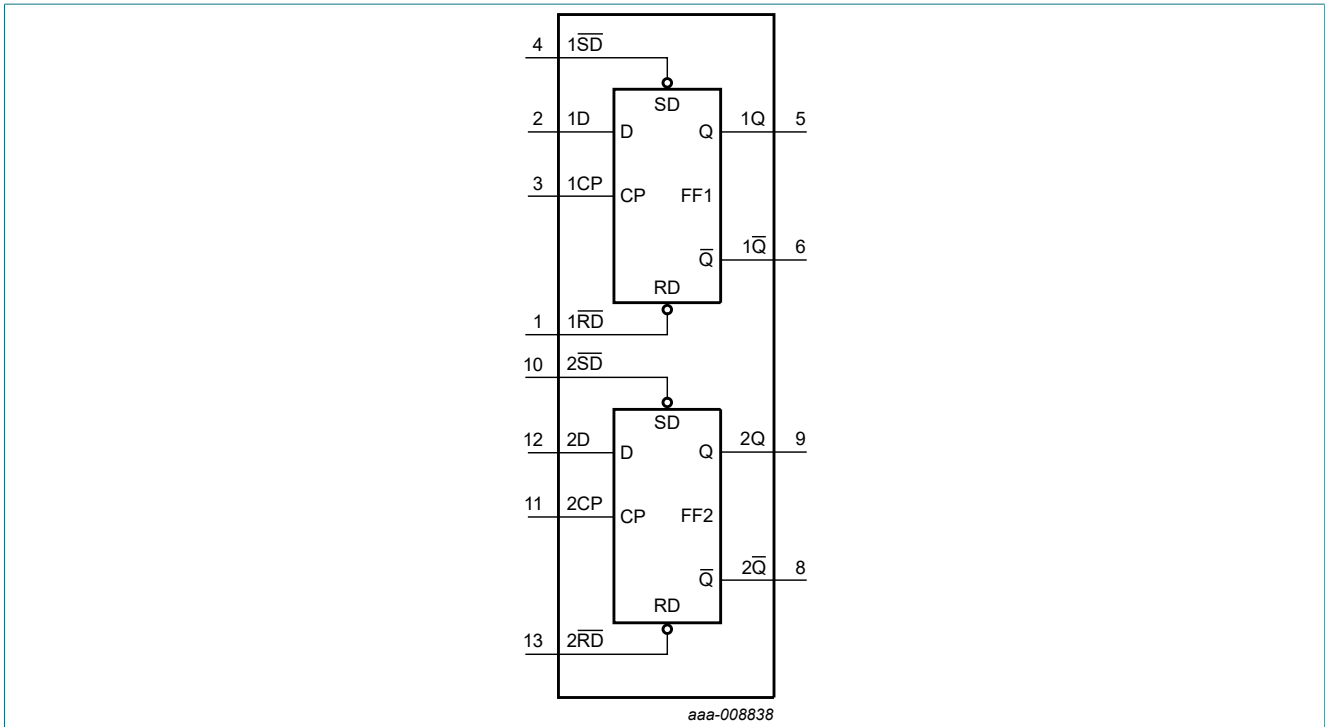


Fig. 3. Functional diagram

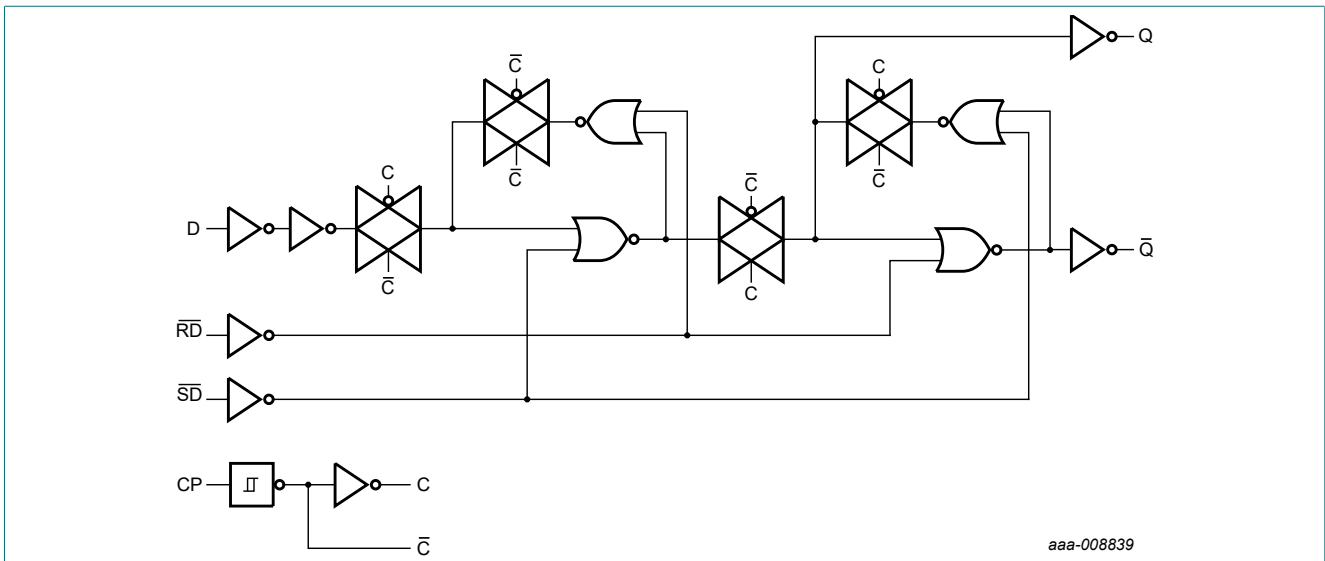


Fig. 4. Logic diagram (one flip-flop)

5. Pinning information

5.1. Pinning

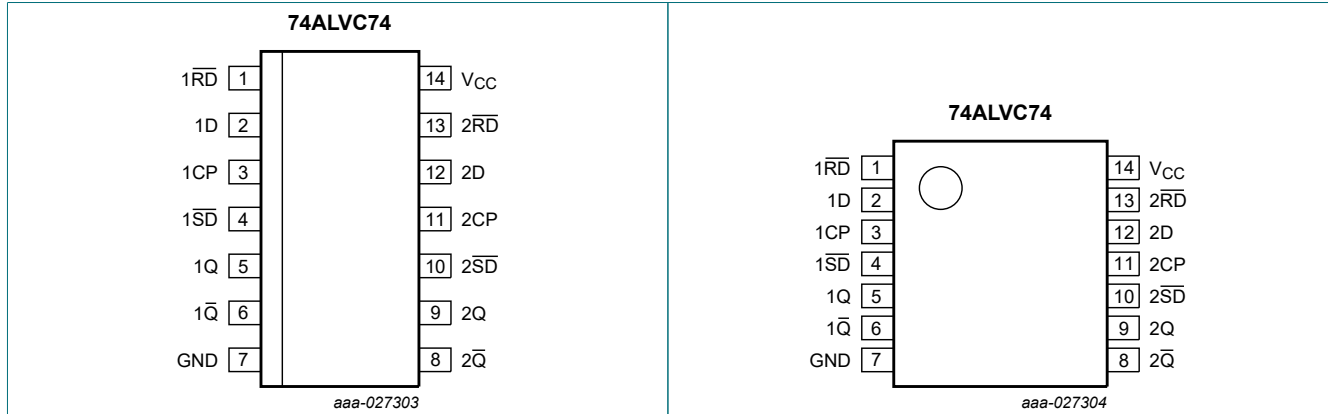
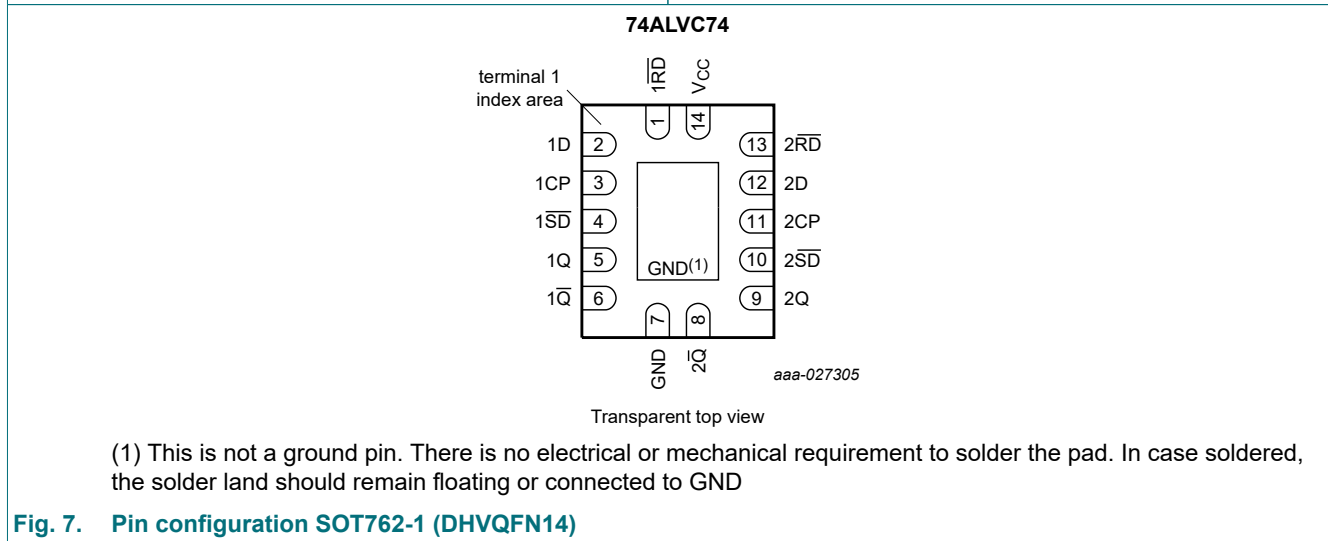


Fig. 5. Pin configuration SOT108-1 (SO14)

Fig. 6. Pin configuration SOT402-1 (TSSOP14)



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND

Fig. 7. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD	1	asynchronous reset-direct input (active-LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH), edge-triggered
1SD	4	asynchronous set-direct input (active-LOW)
1Q	5	true flip-flop output
1Q̄	6	complement flip-flop output
GND	7	ground (0 V)
2Q̄	8	complement flip-flop output
2Q	9	true flip-flop output
2SD	10	asynchronous set-direct input (active-LOW)
2CP	11	clock input (LOW-to-HIGH), edge-triggered
2D	12	data input
2RD	13	asynchronous reset-direct input (active-LOW)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition;
 nQ_{n+1} = state after the next LOW-to-HIGH CP transition

Input				Output			
nSD	nRD	nCP	nD	nQ	nQ̄	nQ _{n+1}	nQ̄ _{n+1}
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		[1] -0.5	+4.6	V
V _O	output voltage		[1] -0.5	V _{CC} + 0.5	V
		Power-down mode; V _{CC} = 0 V	[1] -0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Min	Max	Unit
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	$V_{CC} = 1.65\text{ to }3.6\text{ V}$	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0\text{ V}$	0	3.6	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	20	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$V_{CC} = 1.65\text{ V to }3.6\text{ V}; I_O = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 1.65\text{ V}; I_O = -6\text{ mA}$	1.25	1.51	-	V
		$V_{CC} = 2.3\text{ V}; I_O = -12\text{ mA}$	1.8	2.10	-	V
		$V_{CC} = 2.3\text{ V}; I_O = -18\text{ mA}$	1.7	2.01	-	V
		$V_{CC} = 2.7\text{ V}; I_O = -12\text{ mA}$	2.2	2.53	-	V
		$V_{CC} = 3.0\text{ V}; I_O = -18\text{ mA}$	2.4	2.76	-	V
$V_{CC} = 3.0\text{ V}; I_O = -24\text{ mA}$	2.2	2.68	-	V		

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 1.65 V to 3.6 V; I _O = 100 μA	-	-	0.2	V
		V _{CC} = 1.65 V; I _O = 6 mA	-	0.11	0.3	V
		V _{CC} = 2.3 V; I _O = 12 mA	-	0.17	0.4	V
		V _{CC} = 2.3 V; I _O = 18 mA	-	0.25	0.6	V
		V _{CC} = 2.7 V; I _O = 12 mA	-	0.16	0.4	V
		V _{CC} = 3.0 V; I _O = 18 mA	-	0.23	0.4	V
		V _{CC} = 3.0 V; I _O = 24 mA	-	0.30	0.55	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	±0.1	±5	μA
I _{OFF}	power-off leakage current	V _{CC} = GND; V _I or V _O = 3.6 V	-	±0.1	±10	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	10	μA
ΔI _{CC}	additional supply current	V _{CC} = 3.0 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	750	μA
C _I	input capacitance		-	3.5	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see Fig. 10

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit	
t _{pd}	propagation delay	nCP to nQ, nQ̄; see Fig. 8 [2]					
		V _{CC} = 1.65 to 1.95 V	1.0	3.7	6.2	ns	
		V _{CC} = 2.3 to 2.7 V	1.0	2.6	4.2	ns	
		V _{CC} = 2.7 V	1.0	2.8	4.2	ns	
		V _{CC} = 3.0 V to 3.6 V	1.0	2.7	3.8	ns	
		nSD to nQ, nQ̄; see Fig. 9					
		V _{CC} = 1.65 to 1.95 V	1.0	3.4	5.4	ns	
		V _{CC} = 2.3 to 2.7 V	1.0	2.4	3.8	ns	
		V _{CC} = 2.7 V	1.0	3.2	4.2	ns	
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	3.5	ns	
		nRD to nQ, nQ̄; see Fig. 9					
		V _{CC} = 1.65 to 1.95 V	1.0	3.5	5.4	ns	
		V _{CC} = 2.3 to 2.7 V	1.0	2.5	3.8	ns	
		V _{CC} = 2.7 V	1.0	3.1	4.3	ns	
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	3.5	ns	

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_W	pulse width	nCP; HIGH or LOW; see Fig. 8				
		$V_{CC} = 1.65$ to 1.95 V	2.5	0.9	-	ns
		$V_{CC} = 2.3$ to 2.7 V	2.5	0.6	-	ns
		$V_{CC} = 2.7$ V	2.5	1.3	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	2.5	1.3	-	ns
		nSD or nRD; LOW; see Fig. 9				
		$V_{CC} = 1.65$ to 1.95 V	2.5	0.9	-	ns
		$V_{CC} = 2.3$ to 2.7 V	2.5	0.9	-	ns
		$V_{CC} = 2.7$ V	2.5	1.0	-	ns
$V_{CC} = 3.0$ V to 3.6 V	2.5	0.7	-	ns		
t_{rec}	recovery time	nRD to nCP; see Fig. 9				
		$V_{CC} = 1.65$ to 1.95 V	0.7	-0.2	-	ns
		$V_{CC} = 2.3$ to 2.7 V	0.7	-0.1	-	ns
		$V_{CC} = 2.7$ V	0.7	-0.1	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	0.7	-0.1	-	ns
t_{su}	set-up time	nD to nCP; see Fig. 8				
		$V_{CC} = 1.65$ to 1.95 V	1.2	0.6	-	ns
		$V_{CC} = 2.3$ to 2.7 V	1.2	0.8	-	ns
		$V_{CC} = 2.7$ V	1.1	0.5	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	0.8	0.4	-	ns
t_h	hold time	nD to nCP; see Fig. 8				
		$V_{CC} = 1.65$ to 1.95 V	0.6	-0.4	-	ns
		$V_{CC} = 2.3$ to 2.7 V	0.6	-0.3	-	ns
		$V_{CC} = 2.7$ V	0.7	-0.4	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	0.8	-0.1	-	ns
f_{max}	maximum frequency	nCP; see Fig. 8				
		$V_{CC} = 1.65$ to 1.95 V	150	275	-	MHz
		$V_{CC} = 2.3$ to 2.7 V	200	325	-	MHz
		$V_{CC} = 2.7$ V	250	375	-	MHz
		$V_{CC} = 3.0$ V to 3.6 V	300	425	-	MHz
C_{PD}	power dissipation capacitance	per buffer; $V_I = GND$ to V_{CC} ; $V_{CC} = 3.3$ V [3]	-	35	-	pF

[1] Typical values are measured at $T_{amb} = 25$ °C.

Typical values are measured at $V_{CC} = 1.8$ V for $V_{CC} = 1.65$ V to 1.95 V.

Typical values are measured at $V_{CC} = 2.5$ V for $V_{CC} = 2.3$ V to 2.7 V.

Typical values are measured at $V_{CC} = 3.3$ V for $V_{CC} = 3.0$ V to 3.6 V

[2] t_{pd} is the same as t_{PHL} and t_{PLH} .

[3] C_{PD} is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$, where:

P_D in μ W

f_i = input frequency in MHz;

f_o = output frequency in MHz;

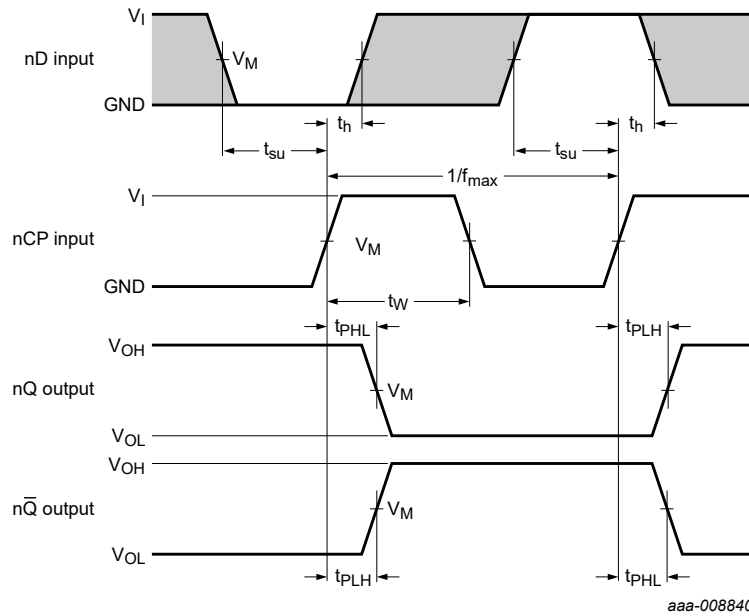
N = total load switching outputs

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

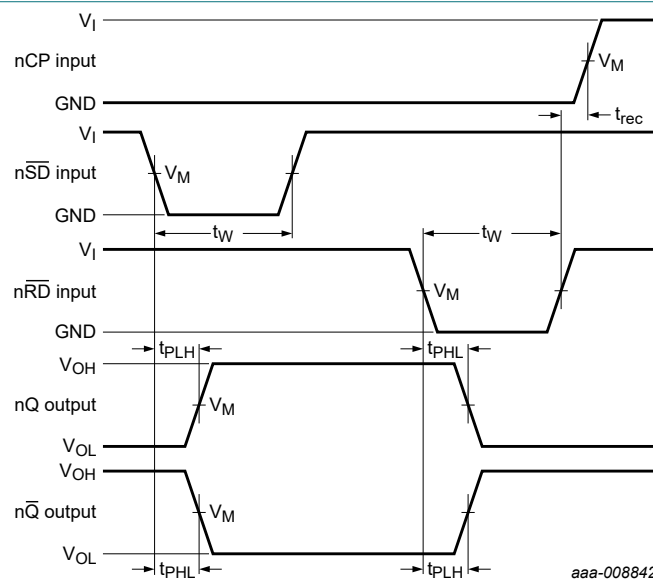
V_{CC} = supply voltage in V.

10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).
 The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 8. Clock pulse (nCP) to output (nQ, nQ̄) propagation delays, nCP pulse width, the nD to nCP set-up times, the nCP to nD hold times and maximum frequency



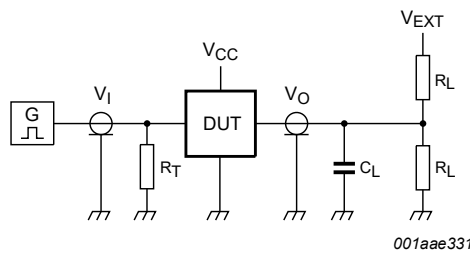
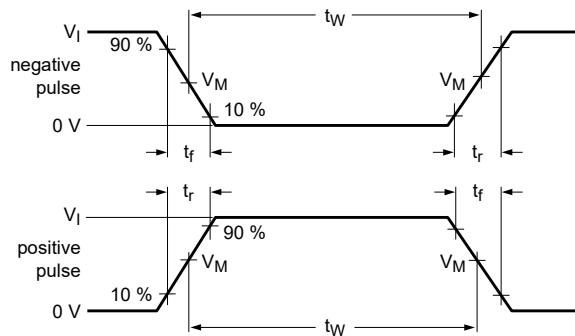
Measurement points are given in [Table 8](#).

Fig. 9. Set (nSD) and reset (nRD) input to output (nQ, nQ̄) propagation delays, set (nSD) and reset (nRD) pulse widths and nRD to nCP recovery time

Dual D-type flip-flop with set and reset; positive-edge trigger

Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.65 V to 1.95 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



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Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 12. Package outline SOT402-1 (TSSOP14)

Dual D-type flip-flop with set and reset; positive-edge trigger

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 13. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC74 v.6	20210727	Product data sheet	-	74ALVC74 v.5
Modifications:	<ul style="list-style-type: none"> Section 10: Minimum set-up time ($t_{su(min)}$) at $V_{CC} = 2.7$ V changed to 1.1 ns. (errata) 			
74ALVC74 v.5	20210430	Product data sheet	-	74ALVC74 v.4
Modifications:	<ul style="list-style-type: none"> Section 2: Reference to JESD36 removed. Section 7: Derating values for P_{tot} total power dissipation have been updated. 			
74ALVC74 v.4	20170816	Product data sheet	-	74ALVC74 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74ALVC74 v.3	20030526	Product specification	-	74ALVC74 v.2
74ALVC74 v.2	20030124	Product specification	-	74ALVC74 v.1
74ALVC74 v.1	20021115	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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