DS26LV31T 3-V Enhanced CMOS Quad Differential Line Driver

1 Features

- Industrial product meets TIA/EIA-422-B (RS-422) and ITU-T V.11 recommendation
- Military product conforms to TIA/EIA-422-B (RS-422)
- Interoperable with existing 5V RS-422 networks
- Industrial and military temperature range
- V_{OD} of 2-V min over operating conditions
- Balanced output crossover for low EMI (typical within 40 mV of 50% voltage level)
- Low power design (330 µW at 3.3V static)
- ESD ≥ 7 kV on cable I/O pins (HBM)
- Specified AC parameter:
  - Maximum driver skew:2 ns
  - Maximum transition time: 10 ns
- Pin compatible with DS26C31
- High Output Impedance in Power-Off Condition
- Available in SOIC packaging
- Standard microcircuit drawing (SMD) 5962-98584

2 Applications

- Motor Control: Brushless DC and Brushed DC
- Field Transmitters: Temperature Sensors and Pressure Sensors

3 Description

The DS26LV31T is a high-speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS26LV31T features low static I_{CC} of 100 µA MAX which makes it ideal for battery powered and power conscious applications.

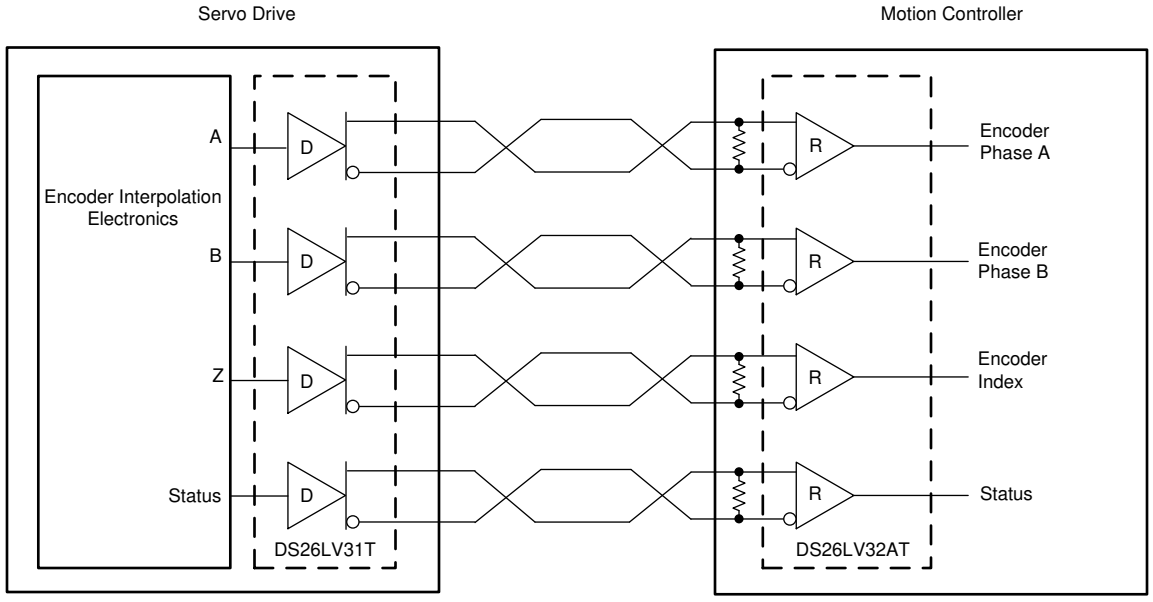
Differential outputs have the same V_{OD} specifies (≥2 V) as the 5 V version.

The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. Protection diodes protect all the driver inputs against electrostatic discharge. Outputs have enhanced ESD protection providing greater than 7 kV tolerance. The driver and enable inputs (DI, EN, EN*) are compatible with low voltage LVTTL and LVCMOS devices.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DS26LV31T	D (16)	9.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2013) to Revision D (June 2020)	Page
• Added Feature: High Output Impedance in Power-Off Condition	1
• Added *Device Information* table, *ESD Ratings* table. *Thermal Information* table, *Feature Description* section, *Device Functional Modes, Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision B (March 1999) to Revision C (February 2013)	Page
• Changed layout of National Data Sheet to TI format	1

5 Pin Configuration and Functions

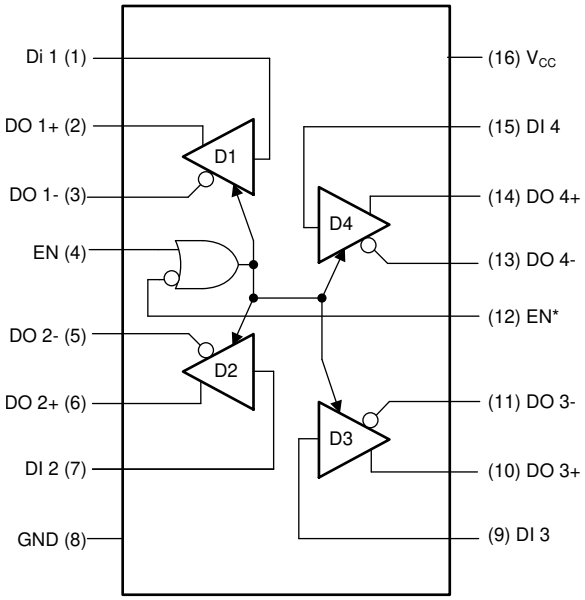


Figure 5-1. Dual-In-Line Package (Top View)

Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
DI 1	1	I	Driver 1 input
DO 1+	2	O	Driver 1 output
DO 1-	3	O	Driver 1 inverted output
EN	4	I	Active high enable
DO 2-	5	O	Driver 2 inverted output
DO 2+	6	O	Driver 2 output
DI 2	7	I	Driver 2 input
GND	8	G	Ground pin
DI 3	9	I	Dirver 3 input
DO 3+	10	O	Driver 3 output
DO 3-	11	O	Driver 3 inverted output
EN*	12	I	Active low enable
DO 4-	13	O	Driver 4 inverted output
DO 4+	14	O	Driver 4 output
DI 4	15	I	Driver 4 input
V_{CC}	16	P	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	−0.5	7	V
EN, EN*	Enable Input Voltage	−0.5	V_{CC}+ 0.5	V
DI	Driver Input Voltage	−0.5	V_{CC}+ 0.5	V
	Clamp Diode Current	−20	20	mA
	DC Output Current, per pin	−150	150	mA
	Driver Output Voltage			
	(Power Off: DO+, DO−)	−0.5	7	V
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Driver output pins	±7000	V
			Other pins	±2500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Free Air Temperature Range	DS26LV31T	−40	25	85	°C
		DS26LV31W	−55	25	125	°C
	Input Rise and Fall Time				500	ns

6.4 Thermal Resistance Characteristics

THERMAL METRIC(1)		DS26LV31T	UNIT
		SOIC (D)	
		16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.5	°C/W
$R_{\theta JC}$	Junction-to-board thermal resistance	31.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS		Pin	MIN	TYP	MAX	UNIT
V_{OD1}	Output Differential Voltage	R_L = ∞ (No Load)		DO+, DO−		3.3	4	V
V_{OD2}	Output Differential Voltage	R_L = 100 Ω (Figure 7-1), I_O ≥ 20 mA			2	2.6		V
ΔV_{OD2}	Change in Magnitude of Output Differential Voltage				−400	7	400	mV
V_{OD3}	Output Differential Voltage	R_L = 3900 Ω (V.11) Figure 7-1 and (3)				3.2	3.6	V
V_{OC}	Common Mode Voltage	R_L = 100 Ω (Figure 7-1)				1.5	2	V
ΔV_{OC}	Change in Magnitude of Common Mode Voltage				−400	6	400	mV
I_{OZ}	TRI-STATE Leakage Current	V_{OUT} = V_{CC} or GND Drivers Disabled				±0.5	±20	µA
I_{SC}	Output Short Circuit Current	V_{OUT} = 0 V, V_{IN} = V_{CC} or GND (4)	T_A = −40°C to +85°C		−40	−70	−150	mA
			T_A = −55°C to +125°C (5)		−30		−160	mA
I_{OFF}	Output Leakage Current	V_{CC} = 0 V, V_{OUT} = 3 V or 6 V				0.03	100	µA
		V_{CC} = 0 V, V_{OUT} = −0.25 V	T_A = −40°C to +85°C			−0.08	−100	µA
			T_A = −55°C to +125°C				−200	µA
V_{IH}	High Level Input Voltage			DI, EN, EN*	2		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}					10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND			−10			µA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA					−1.5	V
I_{CC}	Power Supply Current	No Load, V_{IN} (all) = V_{CC} or GND	T_A = −40°C to +85°C	V_{CC}			100	µA
			T_A = −55°C to +125°C				125	µA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages V_{OD1}, V_{OD2}, V_{OD3}.
(2) All typicals are given for V_{CC} = +3.3 V, T_A = +25°C.
(3) This specification limit is for compliance with TIA/EIA-422-B and ITU-T V.11.
(4) Only one output shorted at a time. The output (true or complement) is configured High.
(5) This parameter does not meet the TIA/EIA-422-B specification.

6.6 Switching Characteristics - Industrial DS26LV31T

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100 Ω, C_L = 50 pF (Figure 7-2 and Figure 7-3)	6	10.5	16	ns
t_{PLHD}	Differential Propagation Delay Low to High		6	11	16	ns
t_{SKD}	Differential Skew (same channel) | $t_{PHLD} - t_{PLHD}$ |			0.5	2	ns
t_{SK1}	Skew, Pin to Pin (same device)			1	2	ns
t_{SK2}	Skew, Part to Part (3)			3	5	ns
t_{TLH}	Differential Transition Time Low to High (20% to 80%)			4.2	10	ns
t_{THL}	Differential Transition Time High to Low (80% to 20%)			4.7	10	ns
t_{PHZ}	Disable Time High to Z	(Figure 7-4 and Figure 7-5)		12	20	ns
t_{PLZ}	Disable Time Low to Z			9	20	ns
t_{PZH}	Enable Time Z to High			22	32	ns
t_{PZL}	Enable Time Z to Low			22	32	ns
f_{max}	Maximum Operating Frequency (4)		32			MHz

(1) f = 1 MHz, t_r and t_f ≤ 6 ns, 10% to 90%.
(2) See TIA/EIA-422-B specifications for exact test conditions.
(3) Devices are at the same V_{CC} and within 5°C within the operating temperature range.
(4) All channels switching, output duty cycle criteria is 40%/60% measured at 50%. This parameter is specified by design and characterization.

6.7 Switching Characteristics - Military DS26LV31W

over operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100 Ω, C_L = 50 pF (Figure 7-2 and Figure 7-3)	5		25	ns
t_{PLHD}	Differential Propagation Delay Low to High	(Figure 7-4 and Figure 7-5)	5		25	ns
t_{SKD}	Differential Skew (same channel) | $t_{PHLD} - t_{PLHD}$ |				5	ns
t_{SK1}	Skew, Pin to Pin (same device)				5	ns
t_{PHZ}	Disable Time High to Z				35	ns
t_{PLZ}	Disable Time Low to Z				35	ns
t_{PZH}	Enable Time Z to High				40	ns
t_{PZL}	Enable Time Z to Low				40	ns

(1) f = 1 MHz, t_r and t_f ≤ 6 ns, 10% to 90%.
(2) See TIA/EIA-422-B specifications for exact test conditions.

6.8 Typical Characteristics

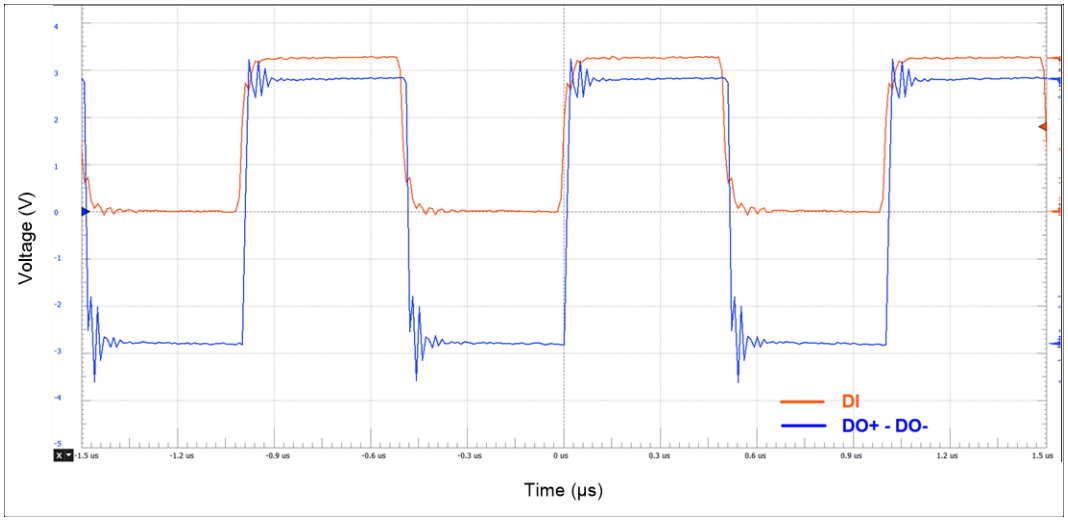


Figure 6-1. Voltage vs Time

7 Parameter Measurement Information

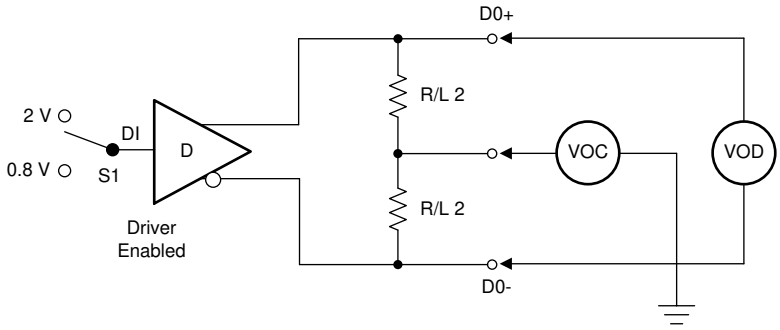


Figure 7-1. Differential Driver DC Test Circuit

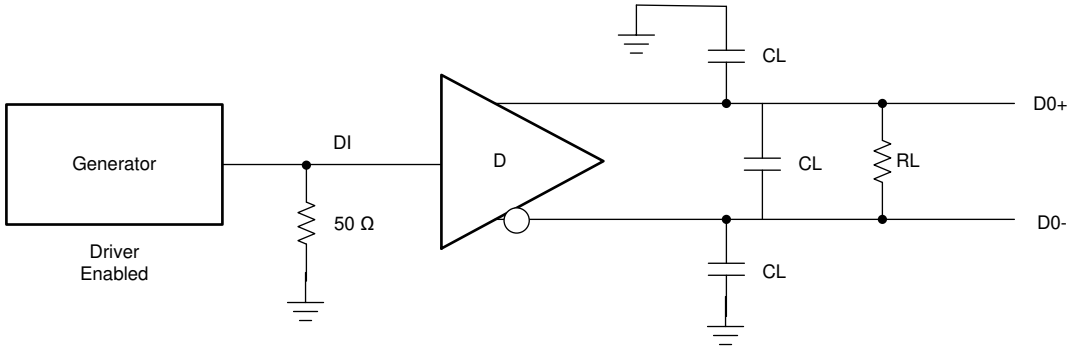
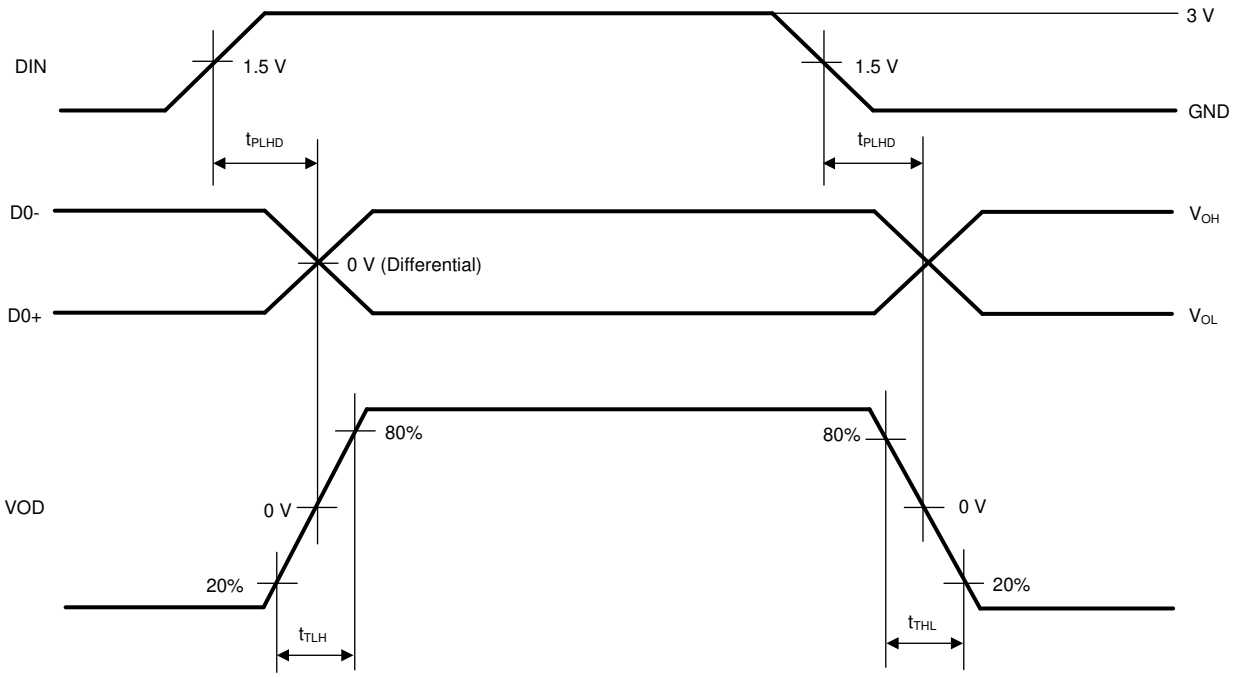
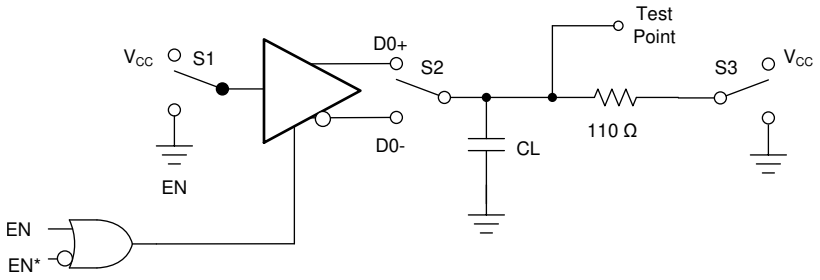


Figure 7-2. Differential Driver Propagation Delay and Transition Time Test Circuit



A. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50% Z_O = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10.
B. C_L includes probe and fixture capacitance

Figure 7-3. Differential Driver Propagation Delay and Transition Time Waveforms



A. If EN is the input, then EN* = High
B. If EN* is the input, then EN = Low

Figure 7-4. Driver Single-Ended TRI-STATE Test Circuit

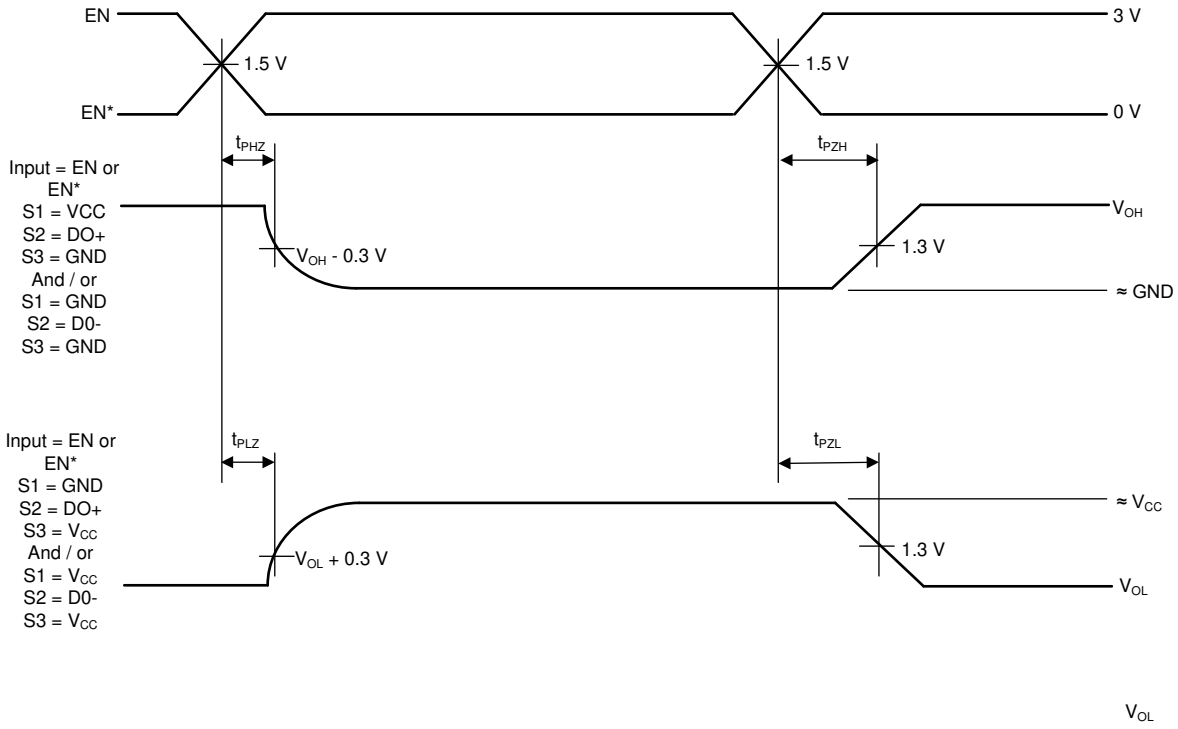


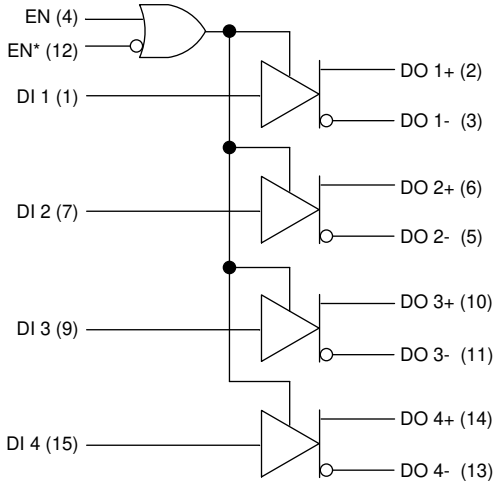
Figure 7-5. Driver Single-Ended TRI-STATE Waveforms

8 Detailed Description

8.1 Overview

The DS26LV31T is a high speed CMOS quadruple differential line drivers with 3-state outputs. The devices are designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 drivers with a single 3.3-V power supply. The drivers also integrate active-high and active-low enables for precise device control.

8.2 Functional Block Diagram



8.3 Feature Description

The devices can be configured using the EN and EN* logic inputs to select transmitter output. A logic high on the EN pin or a logic low on the EN* pin enables the device to operate. These pins are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

The DS26LV31T are optimized for balanced-bus transmission at switching rates up to 32 MHz.

The CMOS DS26LV31T consumes low static I_{CC} of 100 uA MAX that makes it ideal for battery powered applications.

8.4 Device Functional Modes

Table 8-1. Truth Table

Enables(1)		Iput	Outputs	
EN	**EN***	**DI**	**DO+**	**DO-**
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

(1) L = Low logic state, X = Irrelevant, H = High logic state, Z = TRI-STATE

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. If termination is used, it can be placed at the end of the cable near the last receiver. A single driver and receiver, TI DS26LV31T and DS26LV32AT, respectively, were tested at room temperature with a 3.3-V supply voltage. For laboratory experiments, 100 feet of 120-Ω, 24-AWG, twisted-pair cable (Bertek) was used. The communication was succssful with 1Mbps data rate.

9.2 Typical Application

9.2.1 Application

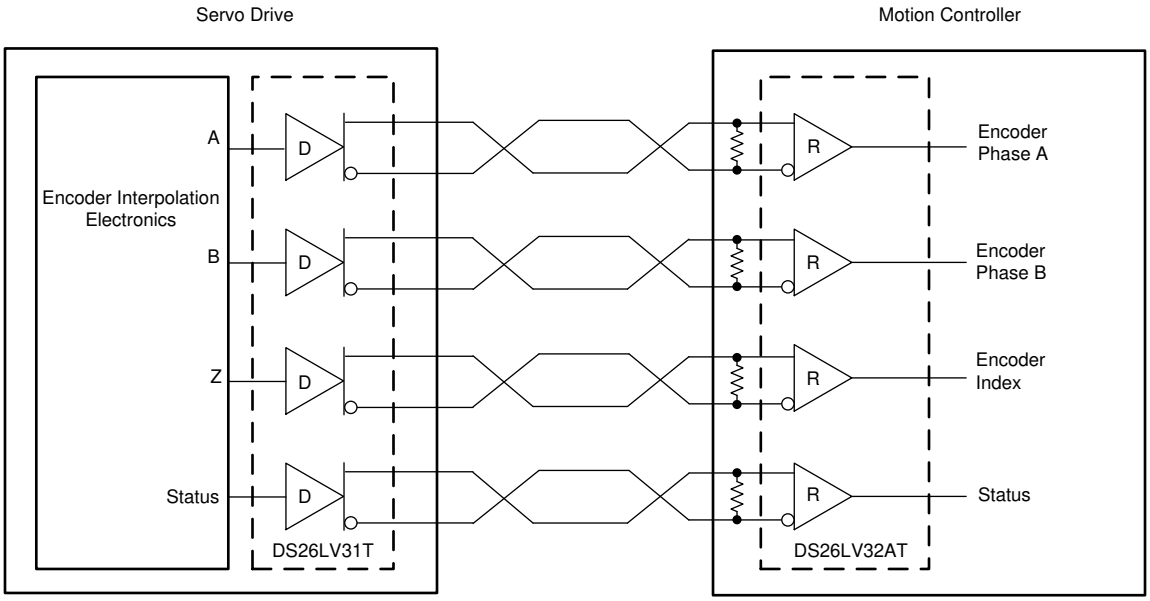


Figure 9-1. Application Schematic - Encoder Application

9.2.2 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, RT, must be within 20% of the characteristic impedance, Zo, of the cable and can vary from about 80 Ω to 120 Ω.

This example requires the following:

- 3.3-V power source
- RS-485 bus operating at 32 MHz or less
- Connector that ensures the correct polarity for port pins

9.2.3 Detailed Design Procedure

Ensure values in Absolute Maximum Ratings are not exceeded. Supply voltage, VIH, and VIL must comply with Recommended Operating Conditions. Place the device close to bus connector to keep traces (stub) short to

prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure 200 mV on the A-B port, if the drive is in high impedance state.

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

- AN-214 Transmission Line Drivers and Receivers for TIA/EIA Standards RS-422 and RS-423
- AN-457 High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Problems
- AN-805 Calculating Power Dissipation for Differential Line Drivers
- AN-847 FAILSAFE Biasing of Differential Buses
- AN-903 A Comparison of Differential Termination
- AN-912 Common Data Transmission Parameters and their Definitions
- AN-916 A Practical Guide To Cable Selection

9.2.3.1 Power Decoupling Recommendations

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 µF in parallel with 0.01 µF at the power supply pin. A 10 µF or greater solid tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

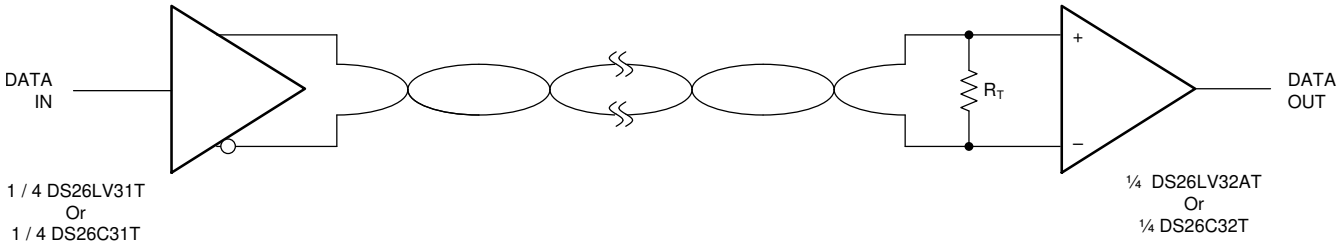


Figure 9-2. Typical Driver Connection - R_T is optional although highly recommended to reduce reflection

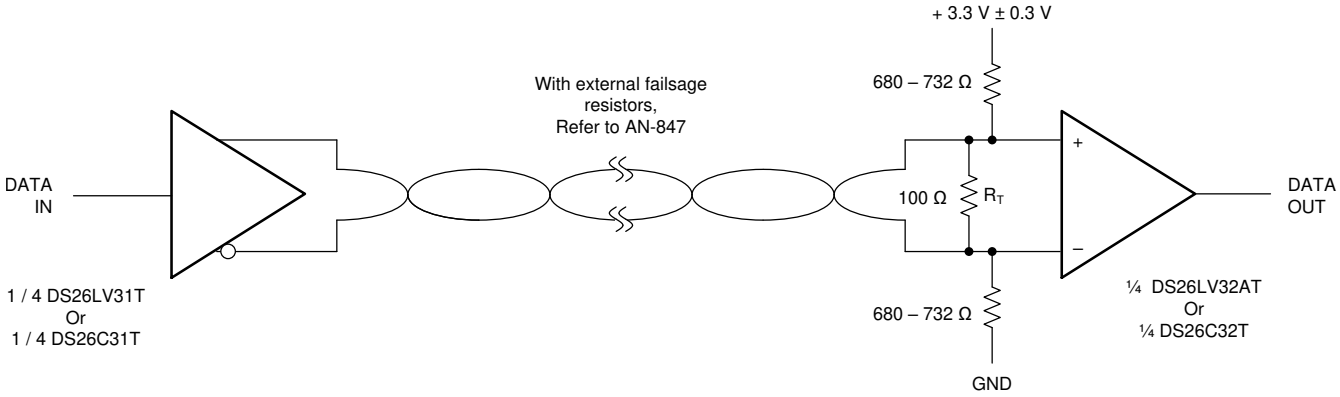


Figure 9-3. Typical Driver Connection

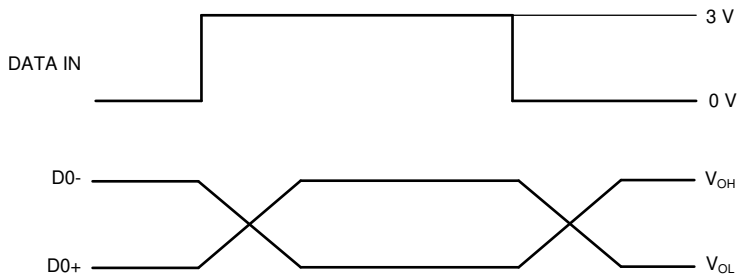


Figure 9-4. Typical Driver Output Waveforms

9.2.4 Application Performance Plots

Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable). The DO measured at the TX end

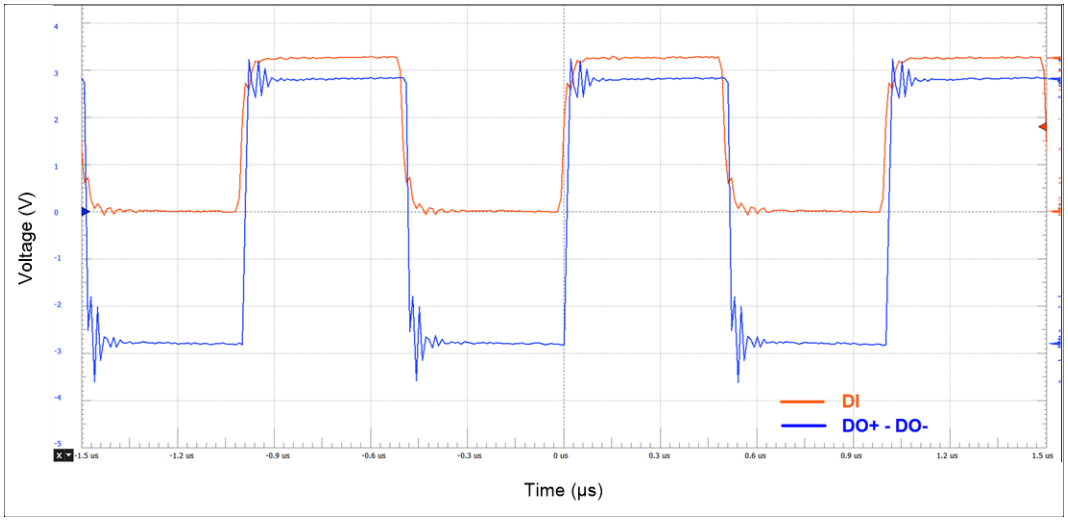


Figure 9-5. Voltage vs Time

10 Power Supply Recommendations

Place a 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry. Connect low-ESR, 0.1-µF ceramic bypass capacitors between supply pin and ground, placed as close to the device as possible.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

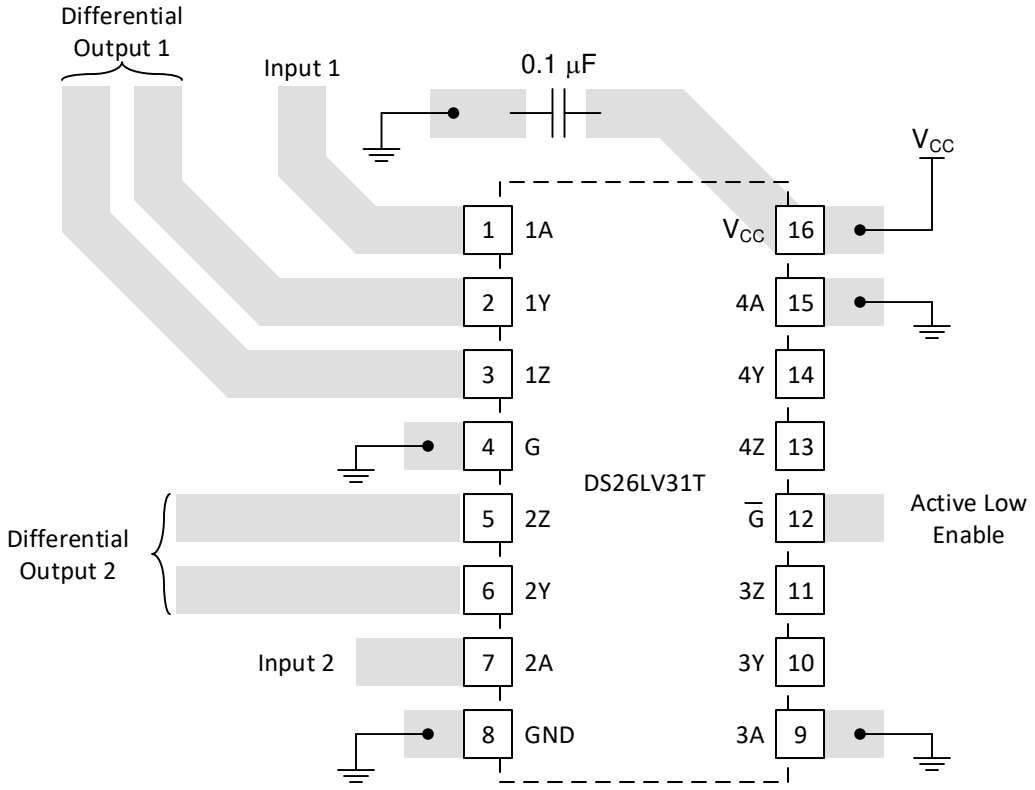


Figure 11-1. Trace Layout on PCB and Recommendations

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26LV31TM/NOPB	ACTIVE	SOIC	D	16	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS26LV31 TM	Samples
DS26LV31TMX/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS26LV31 TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

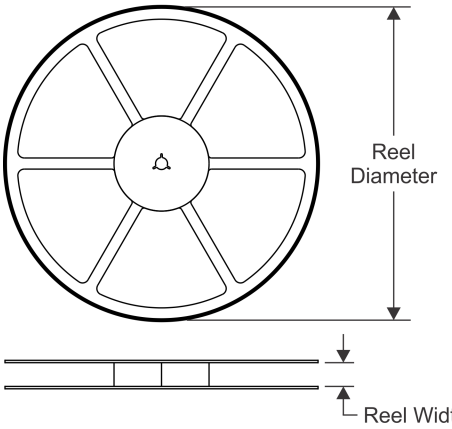
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

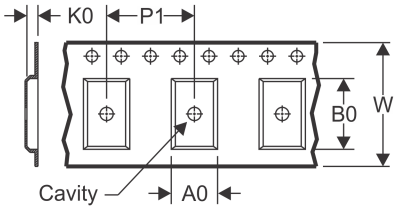
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

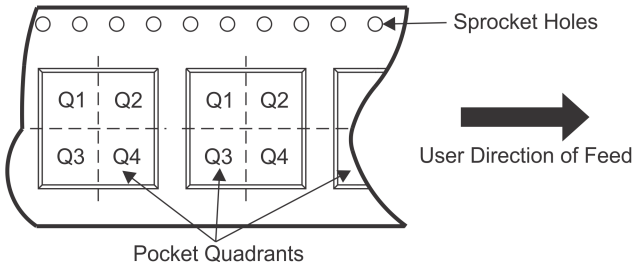


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

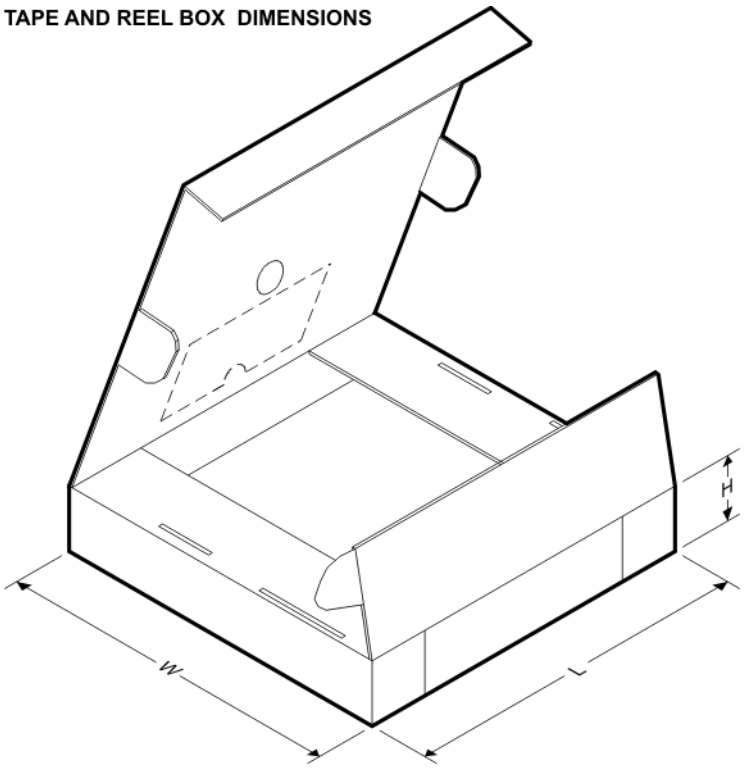
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26LV31TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

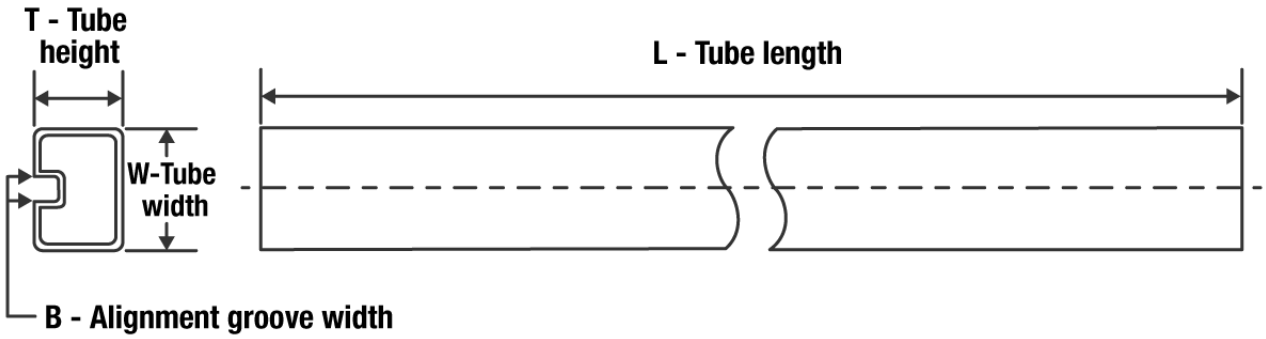
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26LV31TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

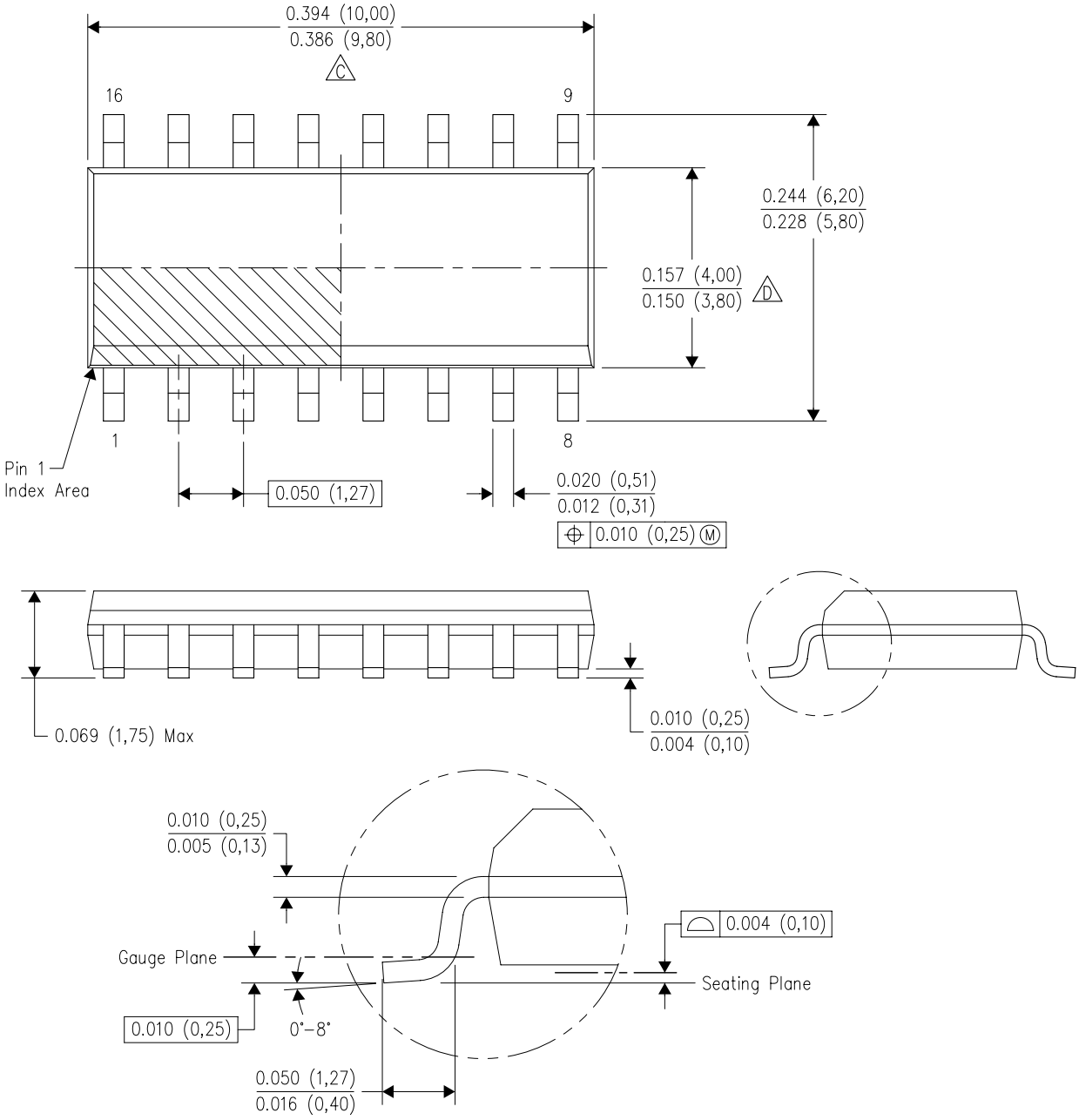
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS26LV31TM/NOPB	D	SOIC	16	48	495	8	4064	3.05

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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