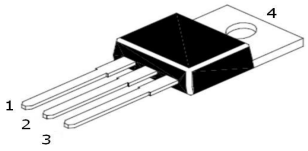
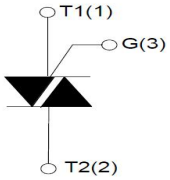
16A TRIACS





BTA16-600/800/1200
TO-220 (Ins)
Plastic Package

BTB16-600/800/1200
TO-220 (Non-Ins)
Plastic Package

BTA16 series triacs, with high ability to withstand the shock loading of large current, provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 quadrant products expecially recommended for use on inductive load.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNIT
Storage junction temperature range		T_{stg}	-40 to 150	°C
Operating junction temperature range		T_j	-40 to 125	°C
Repetitive peak off-state voltage (T_j=25°C)		V_{DRM}	600/800/1200	V
Repetitive peak reverse voltage (T_j=25°C)		V_{RRM}	600/800/1200	V
Non repetitive surge peak Off-state voltage		V_{DSM}	V_{DRM} +100	V
Non repetitive peak reverse voltage		V_{RSM}	V_{RRM} +100	V
RMS on-state current	TO-220 (Ins) (T_C=86°C)	$I_{T(RMS)}$	16	A
	TO-220 (Non-Ins) (T_C=107°C)			
Non repetitive surge peak on-state current (full cycle, F=50Hz)		I_{TSM}	160	A
I^2t value for fusing (t_p=10ms)		I^2t	128	A^2s
Critical rate of rise of on-state current (I_G =2×I_{GT})		dI/dt	50	A/µs
Peak gate current		I_{GM}	4	A
Average gate power dissipation		$P_{G(AV)}$	1	W
Peak gate power		P_{GM}	5	W

ELECTRICAL CHARACTERISTICS (T_j=25°c unless otherwise specified)

3 Quadrants (V_{DRM} /V_{RRM} : 600/800V)

PARAMETER	TEST CONDITIONS	SYMBOL	QUADRANT	VALUES				UNITS
				BW	CW	SW	TW	
Gate Trigger Current	V_D =12V R_L =33Ω	I_{GT}	I - II - III	<50	<35	<10	<5	mA
Gate Trigger Voltage		V_{GT}	I - II - III	<1.3				V
Off-State Gate Voltage	V_D =V_{DRM} T_j =125°C R_L=3.3KΩ	V_{GD}	I - II - III	>0.2				V
Latching Current	I_G =1.2I_{GT}	I_L	I - III	<70	<50	<30	<15	mA
			II	<80	<60	<40	<20	
Holding Current	I_T =100mA	I_H		<60	<40	<25	<15	mA
Critical Rate of Rise of Off-State Voltage	V_D=2/3V_{DRM} Gate Open T_j=125°C	dV/dt		>1000	>500	>200	>100	V/µs

4 Quadrant (V_{DRM}/V_{RRM}: 600/800V)

PARAMETER	TEST CONDITIONS	SYMBOL	QUADRANT	VALUES		UNITS
				B	C	
Gate Trigger Current	V_D =12V R_L=33Ω	I_{GT}	I - II - III	<50	<25	mA
			IV	<70	<50	
Gate Trigger Voltage		V_{GT}	ALL	<1.5		V
Off-State Gate Voltage	V_D =V_{DRM} T_j =125°C R_L =3.3KΩ	V_{GD}	ALL	>0.2		V
Latching Current	I_G =1.2I_{GT}	I_L	I - III - IV	<70	<50	mA
			II	<100	<80	
Holding Current	I_T =100mA	I_H		<60	<40	mA
Critical Rate of Rise of Off-State Voltage	V_D=2/3V_{DRM} Gate Open T_j=125°C	dV/dt		>500	>200	V/µs

3 Quadrants (V_{DRM}/V_{RRM}: 1200V)

PARAMETER	TEST CONDITIONS	SYMBOL	QUADRANT	VALUES	UNITS
Gate Trigger Current	V_D =12V R_L =33Ω	I_{GT}	I - II - III	<50	mA
Gate Trigger Voltage		V_{GT}	I - II - III	<1.5	V
Off-State Gate Voltage	V_D =V_{DRM} T_j =125°C R_L=3.3KΩ	V_{GD}	I - II - III	>0.2	V
Latching Current	I_G =1.2I_{GT}	I_L	I - III	<70	mA
			II	<90	
Holding Current	I_T =100mA	I_H		<60	mA
Critical Rate of Rise of Off-State Voltage	V_D=2/3V_{DRM} Gate Open T_j=125°C	dV/dt		>1500	V/µs

STATIC CHARACTERISTICS

PARAMETER	TEST CONDITIONS		SYMBOL	VALUE (MAX)			UNITS
				-600V	-800V	-1200V	
On-State Voltage	I_{TM} =22.5A t_p=380µs	T_j=25°C	V_{TM}	1.5			V
Off-State Leakage Current	V_D =V_{DRM} , V_R =V_{RRM}	T_j=25°C	I_{DRM}	5	5	10	µA
		T_j=125°C	I_{RRM}	2	2	1	mA

THERMAL RESISTANCES

PARAMETER		SYMBOL	VALUE (MAX)	UNITS
Maximum Thermal Resistance	TO-220 (Ins)	$R_{th(j-c)}$	2.1	°C/W
	TO-220 (Non-Ins)		1.2	

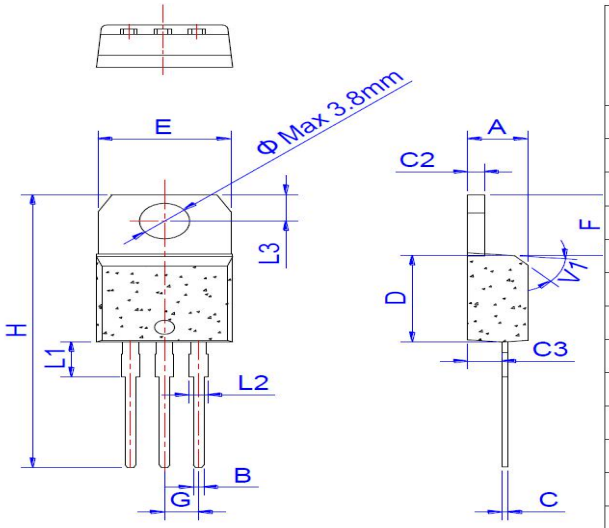
ORDERING INFORMATION

BTA12-XY
BTB12-XY

X = 600: VDRM/VRRM ≥ 600
= 800: VDRM/VRRM ≥ 800
= 1200: VDRM/VRRM ≥ 1200

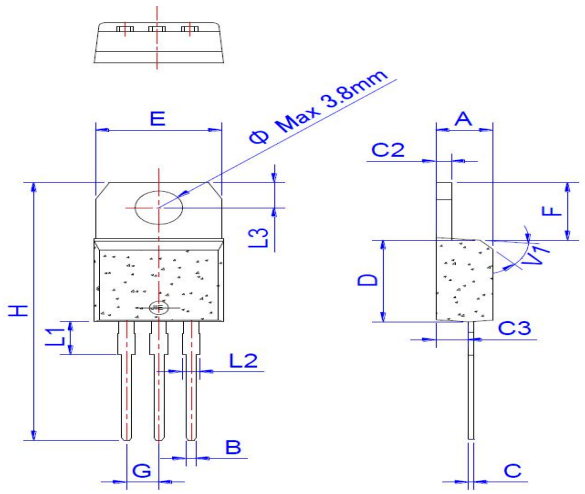
Y = BW: I_{GT1-3} ≤ 50mA
= CW: I_{GT1-3} ≤ 35mA
= SW: I_{GT1-3} ≤ 10mA
= TW: I_{GT1-3} ≤ 5mA
= B: I_{GT1-3}≤50mA I_{GT4}≤70mA
= C: I_{GT1-3}≤25mA I_{GT4}≤50mA

TO-220 (Ins) PACKAGE OUTLINE AND DIMENSIONS



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	0.61		0.88	0.024		0.035
C	0.46		0.70	0.018		0.028
C2	1.21		1.32	0.048		0.052
C3	2.40		2.72	0.094		0.107
D	8.60		9.70	0.339		0.382
E	9.80		10.4	0.386		0.409
F	6.55		6.95	0.258		0.274
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.75			0.148	
L2	1.14		1.70	0.045		0.067
L3	2.65		2.95	0.104		0.116
V1		45°			45°	

TO-220 (Non-Ins) PACKAGE OUTLINE AND DIMENSIONS



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	0.61		0.88	0.024		0.035
C	0.46		0.70	0.018		0.028
C2	1.21		1.32	0.048		0.052
C3	2.40		2.72	0.094		0.107
D	8.60		9.70	0.339		0.382
E	9.60		10.4	0.378		0.409
F	6.20		6.60	0.244		0.260
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.75			0.148	
L2	1.14		1.70	0.045		0.067
L3	2.65		2.95	0.104		0.116
V1		45°			45°	

CHARACTERISTIC CURVES

FIG.1 Maximum power dissipation versus RMS on-state current

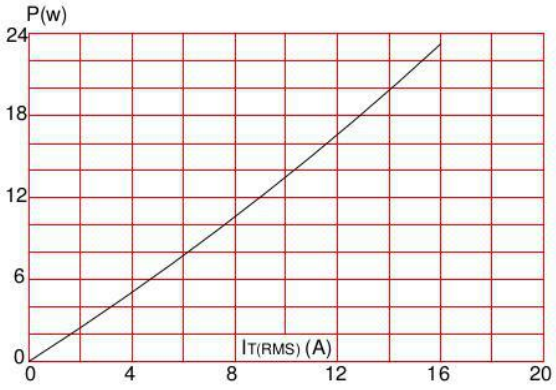


FIG.2: RMS on-state current versus case temperature

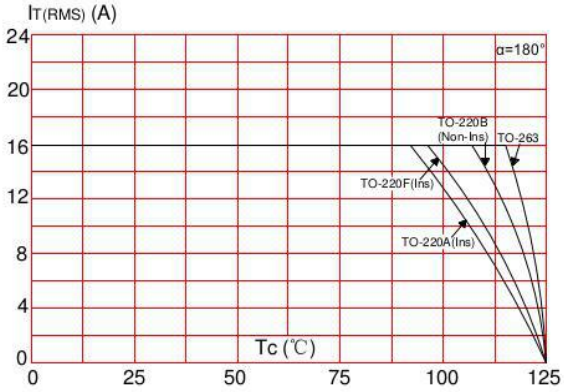


FIG.3: Surge peak on-state current versus number of cycles

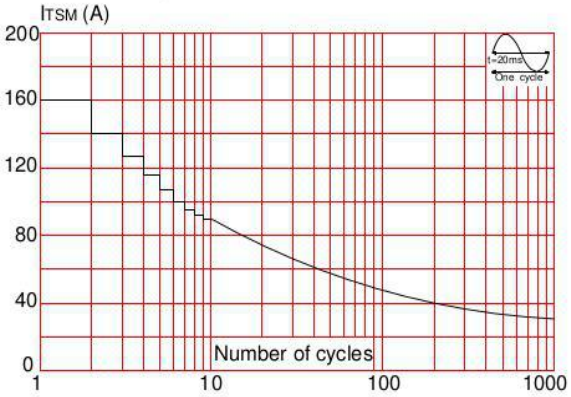


FIG.4: On-state characteristics (maximum values)

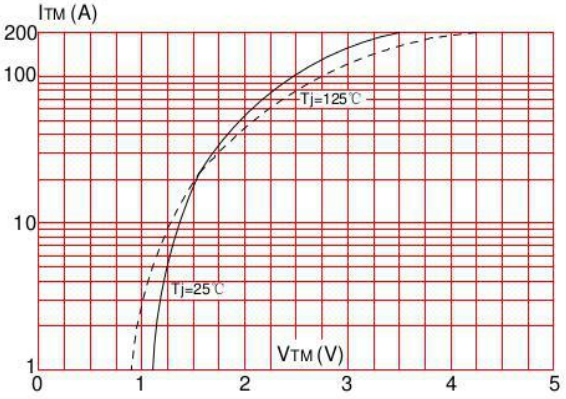


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms, and corresponging value of I^2t (dI/dt < 50A/µs)

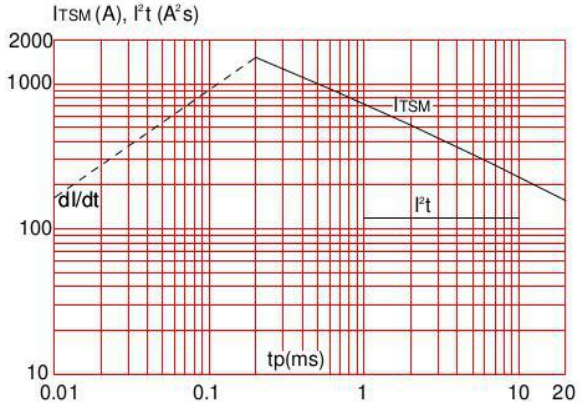
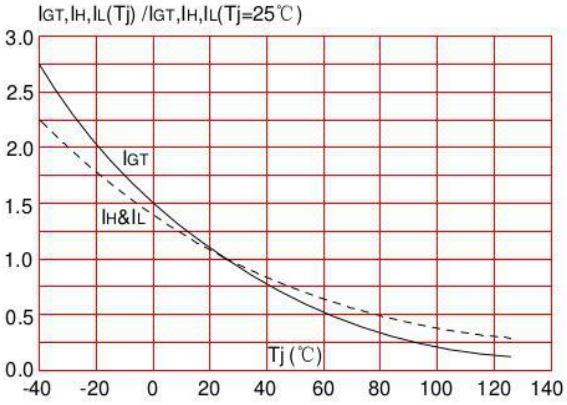


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.

2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

DISCLAIMER

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD is believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.

CDIL is a registered Trademark of
Continental Device India Pvt. Limited
C-120 Naraina Industrial Area, New Delhi 110 028, India.
Telephone + 91-11-2579 6150, 4141 1112 Fax + 91-11-2579 5290, 4141 1119
email@cdil.com www.cdil.com
CIN No. U32109DL1964PLC004291