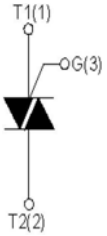
40A TRIACS

BTA41-600/ 800/1200/1600

TOP-3



TOP-3
Leaded Plastic Package
RoHS compliant

FEATURES:

1. High ability to withstand the shock loading of large current
2. Provide high dv/dt rate with strong resistance to electromagnetic interface
3. High commutation performances

APPLICATIONS:

1. On/off function in static relays, heating regulation, induction motor starting circuits
2. Phase control operations in light dimmers,motor speed controllers, and similar applications

ABSOLUTE MAXIMUM RATINGS (T_a = 25 ℃)

PARAMETER	SYMBOL	VALUE	UNIT
Storage junction temperature range	T_{stg}	-40 to 150	°C
Operating junction temperature range	T_j	-40 to 125	°C
Repetitive peak off-state voltage (T_j=25°C)	V_{DRM}	600/800/1200/1600	V
Repetitive peak reverse voltage (T_j=25°C)	V_{RRM}	600/800/1200/1600	V
Non repetitive surge peak Off-state voltage	V_{DSM}	V_{DRM} +100	V
Non repetitive peak reverse voltage	V_{RSM}	V_{RRM} +100	V
RMS on-state current (T_C=80°C)	$I_{T(RMS)}$	40	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I_{TSM}	400	A
I2t value for fusing (t_p =10ms)	I^2t	880	A^2s
Critical rate of rise of on-state current (I_G =2×I_{GT})	dI/dt	50	A/µs
Peak gate current	I_{GM}	4	A
Average gate power dissipation	$P_{G(AV)}$	1	W
Peak gate power	P_{GM}	10	W

ELECTRICAL CHARACTERISTICS at T_a = 25 ℃ (Unless otherwise specified)

3 Quadrants							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**QUADRANT**	**VALUE**			**UNITS**
					BW	**CW**	
Gate Trigger Current	I_{GT}	V_D =12V R_L =33Ω	I - II - III	MAX	50	35	mA
Gate Trigger Voltage	V_{GT}		I - II - III	MAX	1.3		V
Off-State Gate Voltage	V_{GD}	V_D =V_{DRM}, T_j =125°C, R_L =3.3KΩ	I - II - III	MIN	0.2		V
Latching Current	I_L	I_G =1.2I_{GT}	I - III	MAX	80	70	mA
			II		100	80	
Holding Current	I_H	I_T =100mA		MAX	60	50	mA
Critical Rate of Rise of Off-State Voltage	dV/dt	V_D=2/3V_{DRM}, Gate Open Tj =125°C		MIN	1500	1000	V/µs
4 Quadrants							
Gate Trigger Current	I_{GT}	V_D =12V R_L=33Ω	I - II - III	MAX	50		mA
			IV		70		
Gate Trigger Voltage	V_{GT}		ALL	MAX	1.3		V
Off-State Gate Voltage	V_{GD}	V_D =V_{DRM}, T_j =125°C, R_L =3.3KΩ	ALL	MIN	0.2		V
Latching Current	I_L	I_G =1.2I_{GT}	I - III - IV	MAX	90		mA
			II		100		
Holding Current	I_H	IT =100mA		MAX	80		mA
Critical Rate of Rise of Off-State Voltage	dV/dt	VD=2/3VDRM Gate Open	Tj=125°C	MIN	1000		V/µs
Maximum Threshold voltage	V_{TM}	ITM =60A tp=380µs	Tj=25°C	MAX	1.5		V
Pulsed reverse drain current	I_{DRM}	V_D =V_{DRM}	T_j=25°C		10		µA
Maximum reverse leakage current	I_{RRM}	V_R =V_{RRM}	T_j=25°C		5		mA
STATIC CHARACTERISTICS							
On-State Voltage	V_{TM}	ITM =60A, tp=380µs,	Tj=25°C	MAX	1.55		V
Off-State Leakage Current	I_{DRM}	VD =VDRM	T_j=25°C	MAX	10		µA
	I_{RRM}	VR =VRRM	T_j=125°C	MAX	5		mA
THERMAL RESISTANCES							
Junction to case (AC)	$R_{th(j-c)}$				1.1		°C/W

Typical Characteristic Curves

FIG.1 Maximum power dissipation versus RMS on-state current

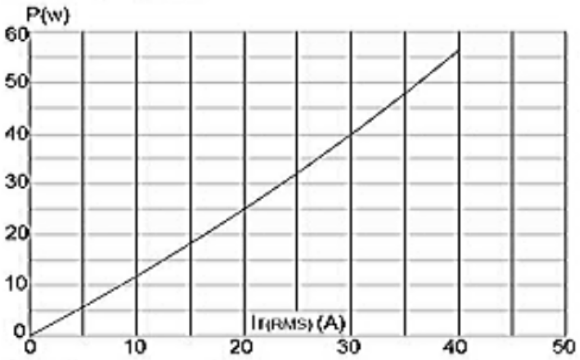


FIG.2: RMS on-state current versus case temperature

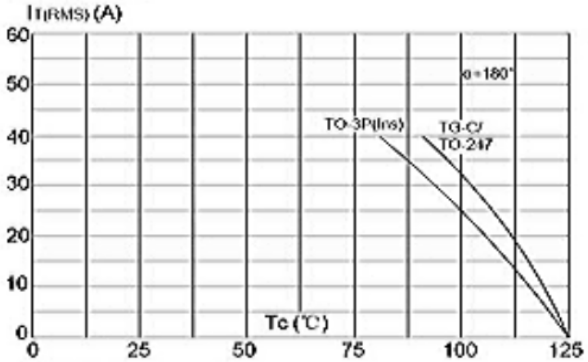


FIG.3: Surge peak on-state current versus number of cycles

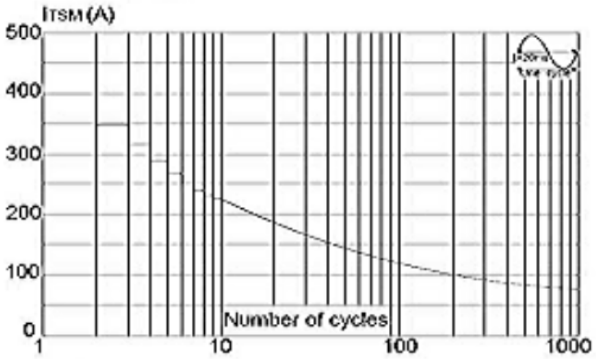


FIG.4: On-state characteristics (maximum values)

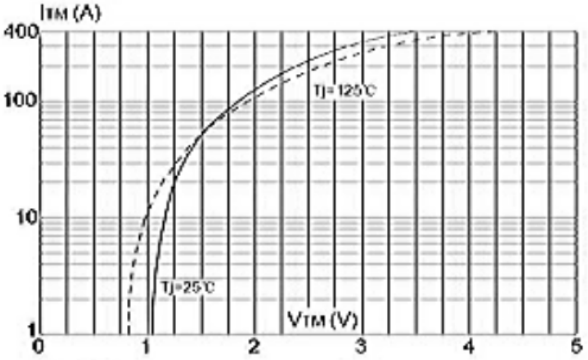


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms, and corresponging value of I²t (dI/dt < 50A/μs)

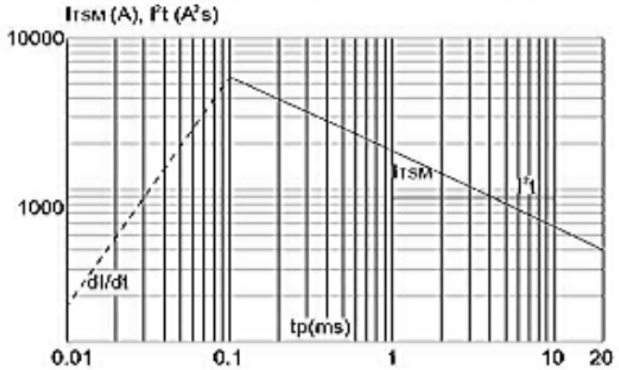
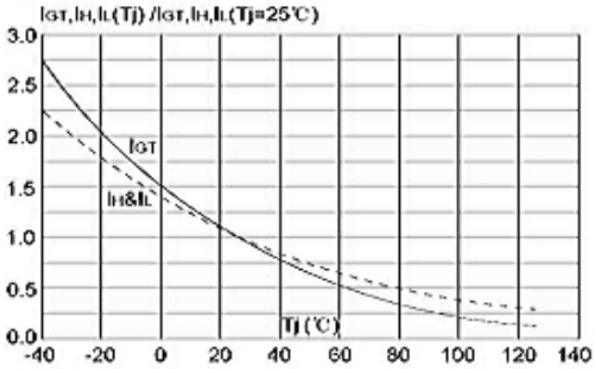
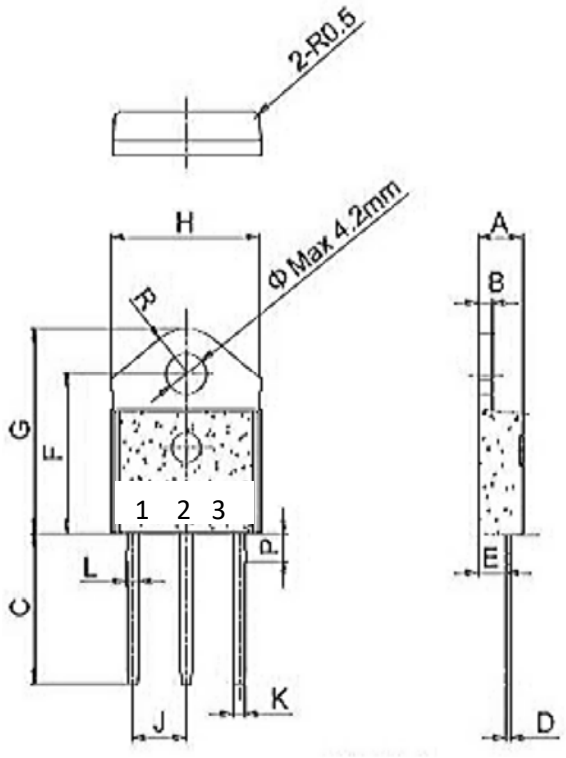


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



Package Details

TOP-3 Leaded Plastic Package



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	1.45		1.55	0.057		0.061
C	14.35		15.60	0.565		0.614
D	0.60		0.70	0.020		0.028
E	2.70		2.90	0.106		0.114
F	15.80		16.50	0.622		0.650
G	20.40		21.10	0.803		0.831
H	15.10		15.50	0.594		0.610
J	5.40		5.65	0.213		0.222
K	1.10		1.40	0.043		0.055
L	1.35		1.50	0.053		0.059
P	2.80		3.00	0.110		0.118
R		4.36			0.171	

Pin Confugration

Pin 1: T1

Pin 2: T2

Pin 3: Gate

Ordering Information

BTA41-XXXX-XX

CW:$I_{GT1-3} \leqslant 35mA$
BW:$I_{GT1-3} \leqslant 50mA$

600:V_{DRM}/V_{RRM}>= 600V
800:V_{DRM}/V_{RRM}>= 800V
1200:V_{DRM}/V_{RRM}>= 1200V

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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CDIL is a registered trademark of
Continental Device India Pvt. Limited
C-120 Naraina Industrial Area, New Delhi 110 028, India.
Telephone +91-11-2579 6150, 4141 1112 Fax +91-11-2579 5290, 4141 1119
email@cdil.com www.cdil.com
CIN No. U32109DL1964PTC004291

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